DC-DC convertors on silicon

next generation technology for emerging business opportunities

new technologies new applications new markets

1st International Workshop on Power Supply on Chip
Clarion Hotel, Cork, Ireland
Sept. 22nd to 24th, 2008

1st International Workshop on Power Supply on Chip

In recent years, power supply miniaturisation and reliability concerns are being increasingly addressed by semiconductor companies through their ability to deliver advanced processing and functional integration in the form of system-in-package (SiP) and system-on-chip (SoC) platforms. This proliferation of functionally-integrated hardware solutions can be seen as an inflection point in the power supply industry which is seeing a dramatic move away from traditional power supply manufacturing (with a focus on the assembly of power supply modules or bricks from discrete components) to an increasing emphasis on power supply products deriving directly from semiconductor and microelectronics products and technologies.

A major challenge to the further miniaturisation of DC-DC converters is the inability to integrate passive components on silicon due to their relatively large size at today's operating frequencies of 0.5 to 5 MHz. Increasing the switching frequencies into the 10 to 100 MHz region offers the potential for the reduction of passive component values to the point where, with the right technology, their size becomes compatible with silicon device dimensions. Currently, significant R&D activity is evident in both academia and industry into advances in semiconductor, magnetic, capacitor and packaging material technologies that will deliver products operating at multi-MHz frequencies. The ultimate target is to develop new miniaturised product formats that can be referred to as power supply-in-package (PSiP) and power supply-on-chip (PwrSoC). This concept of integrated power solutions presents a significant disruptive opportunity in power management solutions and warrants an international forum for its discussion and for the elucidation of the key challenges that lie ahead.

The first International Workshop on Power Supply on Chip will bring together the key players in both the industry and academic communities active in this emerging area. Issues to be addressed include the following:

- ***System Architectures***
- ***Control systems***
- ***Converter Topologies***
- ***Power Trains***
- ***Integrated Capacitors***
- ***Integrated Magnetics***
- ***Market Opportunities***
- ***Power Supply in Package Vs Power Supply on Chip***
- ***Packaging / Functional Integration***
- ***Materials - Magnetic, Capacitor***

Workshop Format: With a targeted audience of 100 to 150 leading academic and industry experts, a workshop format will present an informal forum for the presentation and discussion of up-to-date trends, results, opportunities and challenges. Most importantly, the workshop format will not require speakers to prepare technical papers, enabling a more open forum for the presentation of state-of-the-art results and data.

General Chair: Gerard Hurley, NUI Galway, Ireland.

Programme Chairs: Cian Ó´Mathúna, Tyndall; Francesco Carobolante, Qualcomm

Programme Committee:

Saibal Roy, Tyndall
Arnold Alderman, Anagenesis
Bruno Allard, INSA, Lyon
John Blake, On Semiconductor
José Cobos, UPM, Madrid
Maeve Duffy, NUI Galway
Braham Ferreira, TU Delft
Ray Foley, University College, Cork
Paul McCloskey, Tyndall
Dragan Maksimovic, U. Colorado, Boulder
Joe O'Callaghan, PEIG
Terence O'Donnell, Tyndall
David Perreault, MIT
Fred Roozeboom, NXP Semiconductors
Seth Sanders, Univ. California, Berkeley
John Shen, U. Central Florida
Jeff Sheppard, Darnell
Ed Stanford, Intel
Charles Sullivan, Dartmouth College
Ming Xu, CPES, Virginia Tech
Masahiro Yamaguchi, Tohoku Univ., Japan

Local Organizing Committee:

Cian Ó´Mathúna
Saibal Roy, Tyndall
Julie Dorel, Tyndall
Ningning Wang, Tyndall
Jeffrey Godsell, Tyndall
Ronan Meere, Tyndall
Terence O'Donnell, Tyndall
Paul McCloskey, Tyndall
Jennifer Casey, Tyndall
Brice Jamieson, Tyndall
Fernando M. F. Rhen, Tyndall
Santosh Kulkarni, Tyndall

Programme Schedule

Sunday, September 21st, 2008

17:30 – 19:00

Time	Location	Event
17:30-19:00	Clarion Hotel	Registration

Monday, September 22nd, 2008

08:00 – 09:30

Time	Location	Event
08:00-09:30	Clarion Hotel	Registration
09:00-09:30	Clarion Hotel	Welcome / Opening of Workshop

9.30 – 12.30

Session 1: System Architectures compatible with PwrSoC

Chairs: Ed Stanford, Dragan Maksimovic, José Cobos

Time	Speakers	Affiliation	Country	Title of the talk
PlenaryTalk 9:30-10:15	Fred Lee	CPES	USA	Technology roadmap and survey study for Multi-Hz power conversion
10:15-10:40	Tawfik Arabi	Intel	USA	Power Delivery for the Next Generation Mobile Platforms
10:40-11:15	Poster Presentation, Coffee/Tea Break			
11:15-11:40	David Chesneau, Frederic Hasbani	ST Microelectronics	France	SMPS Integration Challenges - Benefits and Constraints of SMPS Integration in Wireless Multi Media Terminals
11:40-12:05	J. Ted Dibene II	Intel	USA	Integrated Power Delivery for High Performance Server Based Microprocessors
12:05-12:30	Richard Redl	ELFI S.A.	Switzerland	Fundamental considerations for very high frequency power Conversion
12:30-13:30	Clarion Hotel, Lunch			

Programme Schedule

Monday, September 22nd, 2008

13.30 – 16.30

Session 2: Active Semiconductor Device Technologies to Enable PwrSoC

Chairs : John Shen, Ming Xu, John Blake, Bruno Allard

Time	Speakers	Affiliation	Country	Title of the talk
13:30-13:55	Peter Moen	ON Semiconductor	Belgium	High Performance Integrated Power MOSFETs
13:55-14:20	Ettoire Napoli	University of Napoli	Italy	Review of Power IC Technologies
14:20-14:45	John Shen	Univ. Central Florida	USA	Performance Analysis of Lateral and Trench Power MOSFETs for Multi-MHz Switching Operation
14:45-15:15	Poster Presentation, Coffee/Tea Break			
15:15-15:40	Peter Spies	Fraunhofer Institute	Germany	Power Management in Energy Harvesting Power Supplies
15:40-16:05	Patrick Lyle Chapman	University of Illinois	USA	GaN based power converters with integrated passive components
16:05-16:30	Thomas Loeher, Andreas Ostmann	Fraunhofer Institute	Germany	Chip Embedding Technologies for Power Applications
16:30-17:00	Poster Presentation, Coffee/Tea Break			

17.00 – 18.30

Session 3: Open Forum Discussion – Power Supply on Chip Vs Power Supply in Package

Chairs: Francesco Carobolante, Jeff Shepard, Cian Ó Mathúna, Joe O'Callaghan

Time		Event
17:00-18:30		Open Forum Discussion
19:30-20:30	Clarion Hotel	Welcome Reception
20:30-22:30	Clarion Hotel	Dinner

Programme Schedule

Tuesday, September 23rd, 2008

8.30 – 12.20

Session 4: Integrated Passives –A) Magnetics and B) Capacitors

Chairs: Saibal Roy, Terence O'Donnell, Fred Roozeboom, Charles Sullivan, Masahiro Yamaguchi

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4-A) Magnetics:

Time	Speakers	Affiliation	Country	Title of the talk
08:30-08:55	Shan X Wang	Stanford University	USA	Embedded Integrated Inductors with a Single Layer Magnetic Core: Performance Gains and Trade-offs
08:55-09:20	Charles R. Sullivan	Dartmouth College	USA	Losses in laminated thin-film magnetic materials considering displacement current
09:20-09:45	Masahiro Yamaguchi	Tohoku University	Japan	Ferromagnetic integrated inductor/noise suppressor
09:45-10:10	Terence O'Donnell	Tyndall National Institute	Ireland	High efficiency inductors on silicon
10:10-10:40	Poster Presentation, Coffee/Tea Break			

4-B) Capacitors:

Time	Speakers	Affiliation	Country	Title of the talk
10:40-11:05	Magali Brunet	LAAS CNRS	France	3D capacitors on silicon with high density pores network and ZrO2 dielectric films deposited by MOCVD
11:05-11:30	Gordon Grivna, Sudhama Shastri, Yujing Wu, Will Z. Cai	On Semiconductor	USA	A Low Series Resistance, High Density Trench Capacitor for High-Frequency Applications
11:30-11:55	Charles Divita	Gennum Corporation	Canada	Applications, Processing and Integration Options for High Dielectric Constant, Multi-Layer Thin-Film Barium StrontiumTitanate (BST) Capacitors
11:55-12:20	Fred Roozeboom et al	NXP Semiconductors	Netherlands	Ultrahigh-density (> 0.4 μF/mm2) trench capacitors in Silicon
12:20-13:30	Clarion Hotel, Lunch			

Programme Schedule

Tuesday, September 23rd, 2008

13.30 – 16.30
Session 5: Converter topologies and control systems for PwrSoC
Chairs: Dragan Maksimovic, Seth Sanders, Dave Perreault

Time	Speakers	Affiliation	Country	Title of the talk
13:30-13:55	Baoxing Chen	Analog Devices	USA	Fully integrated isolated dc-dc converter and half bridge gate driver with integral power supply
13:55-14:20	Dave Perreault	MIT	USA	Architectures, Topologies and Design Methods for Miniaturized VHF Power Converters
14:20-14:45	Elad Alon	UC Berkeley	USA	Supply Impedance and Voltage Conversion Requirements for CMOS Digital ICs
14:45-15:15	Poster Presentation, Coffee/Tea Break			
15:15-15:40	Eduard Alarcón	UPC Barcelona	Spain	Optimization and implementation of a multi-level buck converter for standard CMOS on-chip integration
15:40-16:05	Seth R. Sanders	UC Berkeley	USA	What about switched capacitor converters?
16:05-16:30	José A. Cobos	UPM Madrid	Spain	Fast dynamics with non linear control: merits and limitations
18:30	Banquet Bus to Blarney from Clarion Hotel			
19:00-23:00	Workshop Banquet			
23:00	Bus to Cork			

Programme Schedule

Wednesday, September 24th, 2008

8.30 – 12.45

Session 6: Monolithic Integration vs System in Package

Chairs: Francesco Carobolante, Paul McCloskey, Braham Ferreira

Time	Speakers	Affiliation	Country	Title of the talk
08:30-08:55	Phil Rutter	NXP Semiconductors	UK	Design Considerations for Integrated Power Trains
08:55-09:20	Matthew Wilkowski	Enpirion	USA	Monolithic Integration Vs "System in a Package"
09:20-09:45	Henk-Jan Bergveld	NXP Semiconductors	Netherlands	Integrated inductive DC/DC down conversion for integrated power management using a two-die approach
09:45-10:10	John S. Glaser	GE Global Research	USA	A 1kW, 330V to 50V DC-DC Power Converter with a 30MHz Switching Frequency
10:10-10:40	Coffee/Tea Break			
10:40-11:05	Arnold Alderman	Anagenesis	USA	Update on PSMA Study of Power Supply in Package Vs Power Supply on Chip - PSiP2PwrSoC
11:05-11:30	J. A. Ferreira	Technical University, Delft	Netherlands	Embedded passives in housing
11:30-11:55	Risto Tuominen	Imbera Electronics	Finland	Embedded Silicon in PCB
11:55-12:20	Ron J. Gutmann	Rensselaer Polytechnic Institute	USA	Smart Power Delivery using Three-Dimensional (3D) IC Technology with Arrays of Monolithic DC-DC Point-of-Load (PoL) Converters
12:20-12:45	Michael A. Briere	International Rectifier Corporation	USA	High-Frequency GaN-Based Power Conversion Stages
12:45-13:00	Close of Workshop			
13:00-14:00	Clarion Hotel, Lunch			

Tyndall Tour (optional)

14:30-15:30	Tyndall National Institute, Welcome, Presentations
15:30-16:30	Tyndall National Institute, Tour

Poster Session:

Monday (September 22nd): 10:40-11:15; 14:45-15:15; 16:30-17:00
Tuesday (September 23rd): 10:10-10:40; 14:45-15:15

1. "***High Efficiency Synchronous Buck Converter using optimised Split-Gate RSO MOSFET***" - C.F. Tong, P.A. Mawby, J. A. Covington, School of Engineering, University of Warwick, Coventry CV4 7AL, UK
   Corresponding author: Dr. C F Tong; Email: c.f.tong@warwick.ac.uk

2. "***An Energy Harvesting System for In-tire TPMS***" - Thomas Herndl - Infineon Technologies Austria AG, Babenbergerstraße 10, A-8020 Graz
   Corresponding author: Dr. Thomas Herndl; Email: thomas.herndl@infineon.com

3. "***High Inductance Density Low Profile Inductor Structure for Integrated DC-DC Converter Applications***" - Qiang Li, Fred C. Lee and David Gilham - Center for Power Electronics Systems (CPES), Virginia Polytechnic Institute and State University, 140 Whittemore Hall, Blacksburg, VA 24061
   Corresponding author: Dr. Qiang Li; Email: lqcpes@gmail.com

4. "***Electrodeposited multilayer amorphous alloy suitable for high frequency integrated inductors***" - Paul McCloskey, Brice Jamieson, Terence O'Donnell, Donald Gardner, Mike Morris, Saibal Roy – Microsystems Center, Tyndall National Institute, UCC, Cork, Ireland
   Corresponding author: Paul McCloskey; Email: paul.mccloskey@tyndall.ie

5. "***3D Integration of Power Supply for Non-isolated Point-of-load Applications***" - Arthur Ball and Fred C. Lee - Center for Power Electronics Systems (CPES), Virginia Polytechnic Institute and State University, 140 Whittemore Hall, Blacksburg, VA 24061
   Corresponding author: Dr. Qiang Li; Email: lqcpes@gmail.com

6. "***LTCC Technology for Low Profile Magnetics Integration***"-Michele Lim, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061, USA.
   Corresponding author: Dr. Michele Lim; Email: mhflim@vt.edu

7. "***Integrated Power Supply Test Methods Enabled with a Dynamic Current Load Module***" - Tom Chambers, Teradyne Inc., Chicago, IL USA
   Corresponding author: Tom Chambers; Email: tom.chambers@teradyne.com

8. "***Optimization of Magnetic Enhancement Layers for High-Frequency Transmission Line Micro-Inductors***" - Brice Jamieson, Terence O'Donnell, Paul McCloskey, D.S. Gardner, Saibal Roy - Microsystems Center, Tyndall National Institute, UCC, Cork, Ireland
   Corresponding author: Brice Jamieson; Email: brice.jamieson@tyndall.ie

9. "***Increasing the Performance of DPWM and A/D Converter for the Future Integrated Power Converters***" - J. Quintero, P. Zumel, C. Fernandez, M. Sanz, A. Lazaro, A. Barrado - GSEP Power Electronics System Group, Universidad Carlos III de Madrid
   Corresponding author: Dr. Pablo Zumel; Email: pzumel@ing.uc3m.es

10. "***Simplifying a Digital Compensator for Integration in PWRSOC and PSIP***" - P. Zumel, C. Fernandez, M. Sanz, A. Lazaro, A. Barrado - GSEP Power Electronics System Group, Universidad Carlos III de Madrid
    Corresponding author: Dr. Pablo Zumel; Email: pzumel@ing.uc3m.es

Poster Session:

Monday (September 22nd): 10:40-11:15; 14:45-15:15; 16:30-17:00
Tuesday (September 23rd): 10:10-10:40; 14:45-15:15

11. "***Characterization of Monolithic Coreless Transformers for Power Supply-on-Chip Applications***"- Rongxiang Wu, Yipeng, Sua, Johnny K.O. Sin, and S.Y. (Ron) Hui, Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong; Department of Electronic Engineering, City University of Hong Kong, Hong Kong
Corresponding author: Prof. Johnny K.O. Sin; Email: eesin@ust.hk ; Dr. WU Rongxiang; Email: wurongxiang@gmail.com

12. "***Micro-fabricated inductors on silicon for DC-DC converters operating at tens MHz***" - Ningning Wang, Terence O'Donnell, Ronan Meere, Santosh Kulkarni, Fernando Rhen, Saibal Roy, Jason Hannon, Raymond Foley, C. O'Mathuna - Microsystems Center, Tyndall National Institute, UCC, Cork, Ireland
Corresponding author: Dr. Ningning Wang; Email: ning.wang@tyndall.ie

13. "***Topology comparison for a system-in-package integrated DC-DC converter for portable electronic applications***" - F. Haizone, J. A. Ferreira (Delft University of Technology), H.J. Bergveld (NXP Semiconductors) and J. Popovic-Gerber (European Centre for Power Electronics).- ECPE, Electrical Power Processing, Mekelweg 4, 2628 CD Delft, The Netherlands
Corresponding author: Dr. Jelena Popović-Gerber; Email: J.Popovic@ewi.tudelft.nl

14. "***On-Chip Bondwire Magnetics with Ferrite-Epoxy Glob Coating for Power Systems on Chip (SOC)***" - Jian Lu, Hongwei Jia, Andres Arias, Xun Gong and Z. John Shen - School of Electrical Engineering and Computer Science University of Central Florida, Orlando, FL 32816, USA
Corresponding author: Dr. John Shen; Email: johnshen@mail.ucf.edu

15. "***A 200-500 mA Monolithic Buck Converter for RF Applications***" - Jason Hannon, Raymond Foley, James Griffiths, Kevin G. McCarthy and Michael G. Egan – Dept. of Electrical Engineering, University College Cork, Ireland
Corresponding author: Jason Hannon; Email: jhannon@pei.ucc.ie

16. "***CoNiFe and CoNiFe-C films for high frequency application***" - Fernando M. F. Rhen, Paul McCloskey, Terence O'Donnell and Saibal Roy - Microsystems Center, Tyndall National Institute, UCC, Cork, Ireland
Corresponding author: Dr. Saibal Roy; Email: saibal.roy@tyndall.ie

17. "***Analysis and Optimization of HF DC/DC Converters for RF Transmitters***" - Malal Bathily[1,2], Frederic Hasbani[1], Bruno Allard[2], [1]STMicrolectronics (Crolles, France), [2]Laboratoire Ampère (Lyon, France).
Corresponding author: Dr. Malal Bathily; Email: malal.bathily@st.com

18. "***Integration of passives components and reliability improvement by design***" - Matthieu Nongaillard; Laboratoire AMPERE UMR CNRS 5005, INSA de Lyon, NXP Semiconductors;
Corresponding author: Dr. M Nongaillard; Email: matthieu.nongaillard@nxp.com

Poster Session:

Monday (September 22nd): 10:40-11:15; 14:45-15:15; 16:30-17:00
Tuesday (September 23rd): 10:10-10:40; 14:45-15:15

19. "***Spiral type micro-inductor with CoNiFe core***" - J.P Laur, D. Bourrier, M. Dilhan, M. Brunet, T.El Mastouli, J.L Sanchez - Université Toulouse, LAAS CNRS, 7 av. du Colonel Roche, F 31077 Toulouse, France.
    Corresponding author: Dr. Monique Dilhan; Email: dilhan@laas.fr
20. "***Nanocomposite mesoporous based materials for application in future inductor cores***" - Jeffrey F. Godsell, Keith P. Donegan, Joseph M. Tobin, Fernando M. F. Rhen, David J. Otway Michael A.Morris, Terence O'Donnell, Justin D. Holmes, Saibal Roy - Microsystems Center, Tyndall National Institute, UCC, Cork, Ireland
    Corresponding author: Dr. Saibal Roy; Email: saibal.roy@tyndall.ie

21. "***Intelligent Power Management Group, University of Limerick: Activities 2008***" - Tony Scanlan, Mark Halton, University of Limerick, Limerick, Ireland
    Corresponding author: Dr. Tony Scanlan; Email: tony.scanlan@ul.ie

22. "***Integrated Passive Components for High Frequency Switching DC-DC Power Converters in Microscale Robots***" - Christopher D. Meyer, Adura Sopeju, Chris Dougherty, Lin Xue, Pengfei Li, Rizwan Bashirullah, and David P. Arnold - Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL 32611, USA
    Corresponding author: Dr. Chris Meyer; Email: toph@ufl.edu

23. "***Integrated Power MEMS Inductor Based on Silicon-Molding Technique***" - Mingliang Wang[1], Khai D. T. Ngo[2] and Huikai Xie[1], [1]Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL 32611, USA; [2]Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, VA 24061, USA
    Corresponding author: Dr. Mingliang Wang; Email: bright80@ufl.edu

24. "***Synchronization Schemes for High Frequency Hysteretic Controlled DC-DC Buck converters***" - Deepak Bhatia, Pengfei Li, Lin Xue, and Rizwan Bashirullah - Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL 32611
    Corresponding author: Dr. Rizwan Bashirullah; Email: rizwan@tec.ufl.edu

25. "***Voltage Scalable Switched Capacitor DC-DC Converters for Ultra-Low-Power On-Chip Applications***" - Yogesh K. Ramadass, Anantha P. Chandrakasan - Massachusetts Institute of Technology, Cambridge, USA
    Corresponding author: Dr. Yogesh K. Ramadass; Email: ryogesh@MIT.EDU

26. "***Loss characterization of magnetic materials for integration on silicon***" - M. Duffy, C. Collins, Power Electronics Research Centre, Dept. of Electronic Engg, NUI Galway, Ireland
    Corresponding author: Dr. Maeve Duffy; Email: maeve.duffy@nuigalway.ie

27. "***Fast response HF DC – DC Converter architecture for RF amplifiers based on a multilevel topology"*** – M. Rodrifuez, J, Sebastian, A. Rodriguez, P.F Miaja, D.G. Lamar, University of Oviedo*, Spain.*
    Corresponding author: Miguel Rodríguez González, Email :rodriguezmiguel.uo@uniovi.es

28. "***Low Parasitic Packaging of Power Modules for High Frequency Operation"*** - Paul McCloskey[a], Ray Foley[b], Virginia Morris[a], Nicolas Cordero[a], Alan Mathewson[a], Cian O'Mathuna[a] ; [a]Tyndall National Institute, Lee Maltings, Cork, Ireland; [b]Department of Electrical Engineering, University College Cork, Ireland Email: alan.mathewson@tyndall.ie

PWR SOC 08 Tyndall National Institute

Session 1: System Architectures compatible with PwrSoC

Monday, September 22nd, 2008 – 9.30 – 12.30

Chairs: Ed Stanford, Dragan Maksimovic, José Cobos

Potential application areas for on-chip or highly integrated power supplies include mobile/battery powered devices, microprocessor power supplies, power management for RF transmitters, energy harvesting, etc. This session addresses the key system-level issues brought out by power supply on chip and other power integration techniques. The session will also discuss the requirements, constraints and trade-offs (i.e. performance, cost, complexity) in such systems with a view to defining the potential benefits of power supply integration. Other issues to be discussed will include: suitable input voltages, single or 2-stage conversion, point of load, integration with load.

Time	Speakers	Affiliation	Country	Title of the talk
PlenaryTalk 9:30-10:15	Fred Lee	CPES	USA	Technology roadmap and survey study for Multi-Hz power conversion
10:15-10:40	Tawfik Arabi	Intel	USA	Power Delivery for the Next Generation Mobile Platforms
10:40-11:15	Poster Presentation, Coffee/Tea Break			
11:15-11:40	David Chesneau, Frederic Hasbani	ST Microelectronics	France	SMPS Integration Challenges - Benefits and Constraints of SMPS Integration in Wireless Multi Media Terminals
11:40-12:05	J. Ted Dibene II	Intel	USA	Integrated Power Delivery for High Performance Server Based Microprocessors
12:05-12:30	Richard Redl	ELFI S.A.	Switzerland	Fundamental considerations for very high frequency power Conversion
12:30-13:30	Clarion Hotel, Lunch			

Abstract 1.1 – Oral Presentation

Plenary Talk:

Survey of Trends for Integrated Point-of-Load Converters

Arthur Ball, Michele Lim, Julu Sun, Qiang Li, Khai D. T. Ngo, Fred C. Lee
Center for Power Electronics Systems (CPES), Virginia Tech, US

Abstract: This survey is targeted at the state-of-the-art technologies and trends toward integration of the point-of-load converters. The survey encompasses an extended literature search ranging from device technologies, magnetic materials, to integration technologies and approaches.
The presentation is organized in three main sections. 1) Device technologies, including Trench MOSFET, Lateral MOSFET and Lateral Trench MOSFET, are discussed with their intended applications. The critical role of device packaging toward high-frequency integration is assessed. An improved Figure -of-Merit (FOM) is proposed to facilitate selection of suitable devices for low-voltage POL applications. 2) Magnetic materials. In recent years, a number of new magnetic materials were explored in various research Labs to facilitate magnetic integration for high-frequency POL applications. These data are collected and organized in such a way to help selecting magnetic material for various current levels and frequency ranges 3) Level of integration are defined with the focus on magnetic integration techniques and approaches, namely board level, package level and wafer level, each with suitable current scale and frequency range.
Finally, an example of 3D integrated POL is presented employing a LTCC magnetic as a substrate and over laid with embedded power layers for integration of active devices. This experiment is aimed at high-density high-current POL. The prototype is demonstrated at 20A and 260W/in3 power density with natural convection cool.

Speaker Biography: Dr. Lee is a University Distinguished Professor at Virginia Tech and Director of the Center for Power Electronics Systems (CPES), a National Science Foundation engineering research center comprised of five universities: Virginia Tech, University of Wisconsin-Madison, Rensselaer Polytechnic Institute, North Carolina A&T University and University of Puerto Rico-Mayaguez as well as 80 industry consortium members. The Center's research vision is to develop an integrated power electronic system approach via an integrated power electronics modular building block concept. Dr. Lee holds 46 U.S. patents and has published over 200 journal articles in refereed journals and more than 525 technical papers in conference proceedings. Among his awards are the William E. Newell Power Electronics Award (1989), the Arthur E. Fury Award for Leadership and Innovation in Advancing Power Electronic Systems Technology (1998) and the Ernst-Blickle Award (2005).

Abstract 1.2 – Oral Presentation

Power Delivery for the Next Generation Mobile Platforms

Tawfik Rahal-Arabi, Fellow IEEE; Hee-Jun Park

Mobile Platform Architecture Development, INTEL Corporation, US

Email: Tawfik.r.Arabi@intel.com

Abstract: Power Delivery has become a key element for the mobile platform to improve battery life and meet the Energy Star requirements. In fact figure 1. shows the power consumption for a typical mobile notebook under Energy Star conditions while figure 2. shows the power consumption under typical battery benchmarks when the LCD is off. It is clear from these figures that power delivery consumes 20% to 50% of platform depending on the benchmark. In addition to this, regulations, especially in the EU, are also accelerating the development of more energy efficient products. Figure 3 shows an example of the increase in environmentally friendly regulations between 2002 and 2007. All of these business and regulatory forces will clearly shape the technology development in the power delivery area.

In this abstract, we will talk about what Intel has been doing at the platform level to improve the energy efficiency of power delivery for the mobile platform, including optimizing for the light load, replacing linear regulators with switching regulators for the LAN, and developing workload dependent architecture for many subsystems on the platform. We will also show measurements of typical systems demonstrating the need for drastic improvements in the notebook power delivery in the next few years.

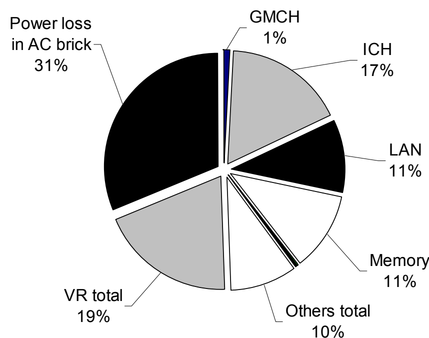


Figure 1: Energy Star consumption by subsystem based a typical notebook platform (S3, LAN cable connected, WOL enabled, internal gfx)

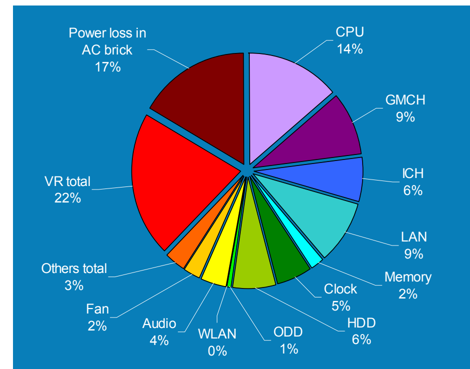


Figure 2: Average Power for a Typical Notebook when the screen is off

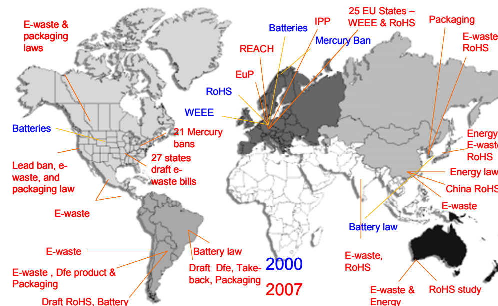


Figure 3: Eco and Energy Efficiency Friendly Regulations in 2007 vs. 2000

Speaker biography:

Dr. Arabi is a senior principal engineer in the Mobility Group at Intel Corporation. He is responsible for defining low power technologies for the next generation notebook platform. His most recent work led to a 30% reduction in power for the mainstream mobile processor built on the 45 nanometers technology.

Dr. Arabi is the recipient of many Intel and IEEE awards including 5 of Intel most prestigious achievement awards given by the executive staff and CEO to only a handful of teams every year. Dr. Arabi is an IEEE fellow and has over 80 Journal and conference publications. He supported and directed research programs between Intel and several leading universities in the US and abroad. Dr. Arabi Graduated from AUB in 1985 with a BS.E.E and a Ph.D from Syracuse University in 1991.

SMPS Integration Challenges: Benefits and Constraints of SMPS Integration in Wireless Multi Media Terminals

David Chesneau and Frederic Hasbani
Wireless Multi Media Division, ST-NXP Wireless
12, Rue Jules Horowitz - BP 217
F-38019 GRENOBLE Cedex France

Abstract: In the context of Multi Media Wireless platform, Switched Mode Power Supplies are today key success factors to achieve high efficiency and extend battery life. However, SMPS compared to classical linear regulators require bulky passive components that significantly increase PCB area and cost. The Graal of platform maker is to reduce passive components size enough to integrate them directly on the silicon die or at least in the same package. In this document, we will review specifications of various SMPS present on Wireless Multi Media platform and analyze how these specifications are compatible or not with integration constraints.

The first part of the study will be dedicated to Digital Base Band applications. We will explain why the accuracy of the power supply is critical to maximize power efficiency of the overall system. Then we will analyze how the constraints on efficiency, accuracy and small external components are compatible. This analysis will help to extract the best trade off for switching frequency and external components values. Finally, with this optimal setup defined, we will evaluate the perspectives of integration in the medium term future.

In the second part, the same exercise will be run in the context of sensitive audio and low power RF applications.The third part will focus on mobile RF Power Amplifiers supply. Since the introduction of spectrally efficient modulations like WCDMA, the SMPS has to provide a wide bandwidth dynamic output to supply the RF PA. Thus, the SMPS is not only a high efficiency energy converter but also an analog signal power amplifier. And the switching frequency must rise according to the desired signal bandwidth, which allows for passive components size reduction and maybe full integration. Moreover, CMOS RF-PA technology requirements are totally compatible with high frequency SMPS implementation: integrating both blocks on a single chip looks like evidence. This offers an additional degree of freedom in the partitioning of a mobile platform. To conclude, our prototype results and design will be presented: a single chip 130MHz SMPS and WCDMA polar reconstruction PA.

Speaker Biography: ***D. Chesneau*** received French engineering diploma from ESIEE (Paris) in 1992 and National Polytechnic Institute of Grenoble in 1998. He joined STMicroelectronics in Grenoble (France) in 1992 as analog designer in the field of video application. From 1994 to 1999, he was involved in the development of high resolution audio sigma delta A/D and D/A converters. Since 1999, he focused on Power Management for mobile phones and mainly on Switched Mode Power Supplies. He currently leads an IP design team specialized in DC/DC converters and he is the author or co-author of several patents in this domain.

F. Hasbani received the Engineering degree in Electronics in 2000 from the National School of Electronics and Radio-Electricity (ENSERG) of Grenoble, France.

He joined STMicroelectronics R&D center in Crolles, France, in 2000. He worked first on analog process compensators and high-speed serial links. His work currently focuses on power management for RF mobile devices, and high frequency SMPS in particular.

Integrated Power Delivery for High Performance Server Based Microprocessors

J. Ted DiBene II
Intel Corporation, Dupont, WA
Joseph.t.dibene.ii@intel.com

Abstract: Microprocessors today are becoming increasingly dense and complex and so is the microprocessor power delivery. Due to the increase in the number of cores per die and the need to selectively operate the processor cores in different modes it has become necessary to segment the power delivery to each core or functional unit block. Moreover, because of the need to reduce power significantly, the power delivery system must delivery power more efficiently and more quickly to the load which necessitates the power conversion be as close to the load as possible, bypassing losses due to parasitic interconnect circuit elements. Thus, integration of the power circuits with the microprocessor package has now become a reality. In order to accomplish this, the power converter must have VLSI type characteristics and be able to scale with the processor needs. The requirements for such a device are clearly challenging and thus integration becomes key to the solution. This presentation discusses some of the challenges with VR level integration on package and how to deliver power to complex loads and segmented rails. The discussion includes an overview of challenges of integrating magnetics and capacitors, parasitics, loadline and guardband effects, and silicon VR power delivery.

Biography: Dr. J. Ted DiBene is currently a lead silicon power architect at Intel. His focus is in power delivery and management for microprocessors and other silicon devices requiring advanced power delivery technologies. Prior to working at Intel, Dr. DiBene was the chief technology officer at INCEP Technologies a startup in San Diego. He has been involved in advanced power delivery research since the late 80's. He is also currently an adjunct professor at the University of Washington. Dr. DiBene holds a BSEE from UC Santa Barbara and MSEE and PhD from UC San Diego. He has 25 patents with numerous pending and has authored many papers in the area of power, signal integrity, and thermal.

Fundamental Considerations for Very High Frequency Power Conversion

Richard Redl
ELFI S.A., Montévaux 14, CH-1726 Farvagny, Switzerland
E-mail rredl@sunrise.ch

Abstract

Dc-dc power converters operating at very high frequencies (between approximately 30MHz and 5 GHz, i.e., in the VHF/UHF band) promise high power density, the possibility of monolithic implementation, and eventually a substantial cost reduction. There is little evidence, however, that increasing the switching frequency beyond a few 10 MHz will lead to those benefits. The main problem is that efficient power conversion in the VHF/UHF range can be achieved only by ZVS operation with very low switching loss. The low switching loss requires the separation of the switch current and voltage transitions, and that can be accomplished only by a complex reactive network (e.g., the one used in a Class E dc-dc converter, Fig. 1). It is difficult to implement such a network on a chip. Furthermore, ZVS operation, and Class E operation in particular, suffers from poor controllability and rapid decrease of the efficiency at reduced load.

This paper will present results of comparisons of the Class E dc-dc converter (a popular choice of researchers for very high frequency power conversion), with selected nonisolated square-wave and resonant converters. The comparisons are based on the concept of the component load factor (Carsten, PCIM 1988) or component stress factor (Wittenbreder, APEC 2006). The analysis shows that compared with the buck converter, at full load the Class E dc-dc converter requires 5 to 10 times more silicon for the same conduction loss (and even more silicon at reduced load). Furthermore, at the same operating frequency the peak stored inductive energy (and consequently the inductor volume) is about 5 to 15 times higher in the Class E converter than in the buck converter.

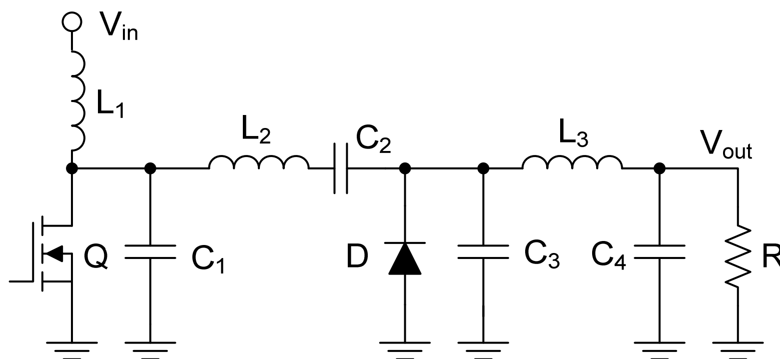


Fig. 1. Class E dc-dc converter

Driving the switch at very high frequencies also presents a difficult challenge. The drive power of a size-optimized MOSFET (Baliga, HFPC 1989) is:

$$P_{drive(min)} = I_{rms} V_G \sqrt{\frac{f}{f_B}}, \quad \text{where} \quad f_B = \frac{1}{R_{ds(on)} C_{in}} \quad \text{and} \quad R_{ds(on)} = \frac{V_G}{I_{rms}} \sqrt{\frac{f}{f_B}}$$

According to the above equations in a Class E converter the drive power of an advanced trench MOSFET at 30 MHz is about 5% of the total output power. Although the drive power can be reduced by various resonant drive techniques, those tend to increase the complexity and further restrict the range of operation. An alternative approach for reducing the drive losses is to use semiconductor devices with inherently higher f_B, e.g. GaAs, GaN, or SiC, but the choice of such devices is very limited.

Considering the additional limitations of the Class E converter, which include the difficulty of implementing good voltage regulation and the poor efficiency at light load it is important to consider alternative, medium-frequency (up to 30 MHz), topologies for high-power-density fully integrated power converter applications. Those topologies might include the ZVS non-inverting buck-boost (U.S. Patent 6,788,033), some quasi-resonant, multi-phase and multi-level converters, and also isolated converters, including the Class $(DE)^2$ converter (Hamill, PESC 1996) and the sine amplitude converter (U.S. Patent 9,930,893). The paper will conclude with an overview and fundamental evaluation of the most promising converter topologies.

Speaker Biography

Richard Redl received the diploma in telecommunications engineering in 1969 and the Technical Doctor degree in 1973, both from the Technical University of Budapest, Hungary. Since 1990 he is a consultant in Switzerland, specializing in power electronics. He holds three Hungarian and nineteen U.S.A. patents, has written over hundred technical papers, and is a co-author of a book on dynamic analysis of power converters. Dr. Redl is a Fellow of the IEEE.

PWR SOC '08 | Tyndall National Institute

Session 2: Active Semiconductor Device Technologies to Enable PwrSoC

Monday, September 22nd, 2008 – 13.30 – 16.30

Chairs: John Shen, Ming Xu, John Blake, Bruno Allard

This session discusses active switching power devices suitable to facilitate various PwrSoC concepts, ranging from traditional BCDMOS to vertical/lateral hybrid devices and SOI RESURF devices. The focus will be on multi-MHz and RF operation, process compatibility, and special power electronics requirements such as SOA and energy capability of different CMOS-based device technologies.

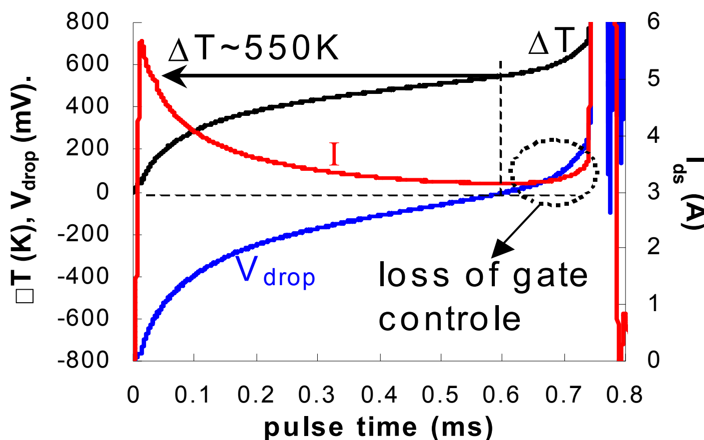
Time	Speakers	Affiliation	Country	Title of the talk
13:30-13:55	Peter Moen	ON Semiconductor	Belgium	High Performance Integrated Power MOSFETs
13:55-14:20	Ettoire Napoli	University of Napoli	Italy	Review of Power IC Technologies
14:20-14:45	John Shen	Univ. Central Florida	USA	Performance Analysis of Lateral and Trench Power MOSFETs for Multi-MHz Switching Operation
14:45-15:15	Poster Presentation, Coffee/Tea Break			
15:15-15:40	Peter Spies	Fraunhofer Institute	Germany	Power Management in Energy Harvesting Power Supplies
15:40-16:05	Patrick Lyle Chapman	University of Illinois	USA	GaN based power converters with integrated passive components
16:05-16:30	Thomas Loeher, Andreas Ostmann	Fraunhofer Institute	Germany	Chip Embedding Technologies for Power Applications
16:30-17:00	Poster Presentation, Coffee/Tea Break			

High Performance Integrated MOSFETs

P. Moens and M. Tack

Power Technology Centre, Corporate R&D
ON Semiconductor, Belgium, Westerring 15, B-9700 Oudenaarde, Belgium
Tel : +32-55-332471 ; E-mail : peter.moens@onsemi.com

Abstract: This presentation on High Performance Integrated MOSFETs will detail on the integration aspects of power drivers in advanced submicron CMOS technologies. These so-called Smart Power Technologies try to incorporate some level of power handling capability on-chip, with voltages in the 50 to 150V range, and current levels up to 6-8 Amps. Applications are typically in automotive, industrial and high voltage communication (power-over-ethernet). In a first part of the presentation, the trend of node scaling on smart power technologies is discussed and compared to the well-known ITRS roadmap for CMOS. Next, the different technology options for integration of high voltage drivers will be discussed. The specifics of matrix technologies, BCD technologies and SOI are given. The competition landscape in these three different technological fields is presented.
A second part of the presentation highlights the different device concepts that are used in industry to make high performance integrated MOSFETs. The lateral resurf lateral DMOS (rLDMOS), the quasi-vertical DMOS (Q-VDMOS) as well as the trench-based MOS (TB-MOS) are presented and integration aspects and performance are discussed. Special attention is devoted to the total Safe Operating Area (SOA) of such power drivers. The concept of electrical, thermal and hot carrier SOA is presented. The electrical SOA determines the boundary conditions in current and voltage within which the power driver can be operated without triggering of the intrinsic parasitic bipolar transistor by electrical effects i.e. by applying short pulses (e.g. a system ESD event). Likewise, the thermal SOA is determined by the triggering of the parasitic bipolar by thermal effects due to long power pulses (e.g. inductive switching). The concept of "critical temperature T_{crit}" is introduced, and experimental validation of T_{crit} is provided. Upon triggering of the bipolar, gate control is lost and the power device is destructed by thermal run-away, see the figure below. On the other hand, hot carrier effects will slowly degrade the Si/SiO_2 interface, and cause a gradual shift of the transistor parameters, without causing hard failure. The three different device types (rLDMOS, Q-VDMOS, TB-MOS) are compared with respect to their total SOA.
Finally, the electrical isolation of power drivers from the CMOS circuitry by deep trenches is detailed.



Biographies

Peter Moens received a M.Sc. and a Ph.D. in solid state physics from the University of Gent, Belgium, in 1990 and 1993 respectively.
From 1993 till 1996, he worked as a post-doctoral fellow in collaboration with Agfa-Gevaert, Mortsel Belgium on the electron capture efficiency of silver halide emulsions. In 1996, he joined ON Semiconductor, Belgium where he is involved in the technology and device development for power applications. His fields of interest are novel device concepts and reliability related aspects of integrated smart power devices such as hot carrier degradation and ESD issues. He is author or co-author of over 100 papers in international scientific journals and in international conference proceedings, and has issued over 10 patents in his field of application.
Dr. Moens is member of the technical program committee of ISPSD, IRW, ESREF and the ESD/EOS Symposium, and serves as the chair of the HV reliability subcommittee of IRPS. He also serves as the technical program chair of ISPSD2009. He is also Guest Editor of IEEE Transactions on Devices and Material Reliability.

Marnix Tack received the M.Sc. degree in electrical engineering from the University of Gent, Belgium, in 1984, and the Ph.D. degree from the Catholic University of Leuven, Belgium in 1991. He joined IMEC in 1985 working in the field of SOI-CMOS.
He joined Mietec in 1990, that later became Alcatel MicroElectronics, and was then acquired by AMIS in 2002 which finally become ON Semiconductor in 2007. He started as a technology Projectleader where he developed C07, then became Production Manager of the Testing Operations in Oudenaarde, and subsequently took a 1yr assignment as a full-time "coach" to reengineer several departments (Fab Operations, Engineering, IT). In 1996 he was promoted to Technology Director and later World Wide Senior Director of Technology R&D after the AMIS acquisition. He managed programs on CMOS, SiGe-BiCMOS, NVM (OTP, EE, Flash), and especially Smart Power, where he initiated and managed the development of the I3T platform. He also managed several technology transfers, including outsourcing operations with leading foundries like TSMC and UMC. He (co-)authored over 60 publications and served on the technical committee of ESSDERC and ISPS.

Abstract 2.2 – Oral Presentation

Review of Power IC Technologies

Ettore Napoli
University of Napoli
Italy

Abstract: The talk reviews the current status of lateral power semiconductor devices and technologies for high voltage integrated circuits (HVICs) and discusses new trends in the field.

The first part of the talk introduces Dielectric Isolation, Junction Isolation and SOI as techniques for the manufacture of lateral power devices.

The second part introduces the resurf effect showing the examples of 1D, 2D and multipe RESURF technologies.
The RESURF and concept is presented and compared with the vertical Superjunction (SJ) concept and the use of field plates to improve the breakdown performance of power devices.
This allows to present the different technologies under a common unifying theory and allows an in depth comprehension of device behaviour.

New forms of RESURF concepts and state of the art silicon technologies are presented in the conclusions.
As example 3D RESURF, thin silicon and unbalanced Superjunction are considered. High voltage Silicon on Insulator (SOI), based on the membrane technology that allows almost ideal Breakdown voltage for lateral power devices, and deep depletion concept for SOI devices, that introduces the concept of transient breakdown voltage, are also presented.

Speaker biography: Ettore Napoli was born in, Italy, in 1971. He is associate Professor at the University of Napoli since 2005. He did Ph.D. in Electronic Engineering in 1999. Electronic engineering degree with honors in 1995; Research Associate at the Engineering Dept. of the University of Cambridge (UK) in 2004.

His scientific interests include modeling and design of power semiconductor devices and VLSI circuit design. In the power devices field his main interests are the PiN diode, the vertical IGBT, superjunction devices and Lateral IGBT on SOI substrate.
In the VLSI field his interests are high speed arithmetic circuits and advanced flip-flops.

Prof. Napoli is author or co-author of more than fifty paper published in international journals and conferences.

Abstract 2.3 – Oral Presentation

Performance Analysis of Lateral and Trench Power MOSFETs for Multi-MHz Switching Operation

John Shen
School of Electrical Engineering & Computer Science University of Central Florida

Abstract: This talk presents a comparative study of lateral and trench power MOSFETs in hard switching synchronous buck converters operating in the multi-MHz frequency range based on a mixed-mode device/circuit modeling approach. Detailed power loss analysis is performed for the control and synchronous MOSFETs. It is observed that the inherently low gate charge QG of lateral MOSFETs offers significant reduction in gate drive losses, which become increasingly important in the multi-MHz frequency range and especially light load conditions. Furthermore, the power loss due to the reverse recovery of the SyncFET body diode becomes a major limiting factor in the MHz frequency range for both trench and lateral MOSFETs. This factor will eventually determine the maximum practical switching frequency of the buck converter.

Biography: Dr. John Shen is an Associate Professor of Electrical Engineering and director of Power Semiconductor Research Lab at the University of Central Florida (UCF). He received his BSEE from Tsinghua University (China) in 1987, MS and PhD both in electrical engineering from Rensselaer Polytechnic Institute (USA) in 1991 and 1994, respectively.
Dr. Shen's research areas include power electronics, power semiconductor devices and ICs, and renewable and alternative energy systems. He has published over 80 journal and conference articles, and holds 9 issued and many pending US patents in these areas. He is the inventor of the world's first commercial sub-miliohm power MOSFET. He is a recipient of the 2003 NSF CAREER Award, the 2006 IEEE Prize Paper Award from IEEE Society of Power Electronics, the 2003 IEEE Best Automotive Electronics Paper Award from IEEE Society of Vehicular Technology, and the 1996 Motorola Science and Technology Award. He served as the Technical Program Chair of PESC07. He currently chairs the Power SemiconductorsTechnical Committee of the IEEE Power Electronics Society.

Power Management in Energy Harvesting Power Supplies

Peter Spies, Nordostpark 93, 90411 Nuremberg, Germany
Phone ++49(0) 0911 / 58061 6363
Email: peter.spies@iis.fraunhofer.de
www.iis.fraunhofer.de
www.smart-power.fraunhofer.de

The presentation introduces a design study on power management ICs for energy harvesting power supplies. Relevant specifications are derived from properties of energy sources in the daily environment. Main design goal is low supply voltage (start-up voltage) and high efficiency. Functional circuit blocks and schematic examples for dc-dc converters and maximum power point trackers are discussed. These circuits ensure the maximum output power from the energy transducers like thermo-generators, solar cells or kinetic transducers independent of the environmental conditions. Additional circuitry and functionalities required for the operation in autonomous systems like wireless sensors will be introduced. The special focus of low power consumption and low leakage currents is discussed against the background of the development of semiconductor technologies. Simulation results of integrated circuit blocks and measurements from practical realizations are presented. Finally, a hardware demonstrator for wireless data transmission powered by the heat of the human hand is introduced. A dc-dc converter with a start-up voltage of 100 mV enabled by a self-oscillating coupled inductors architecture is used in this demonstrator.

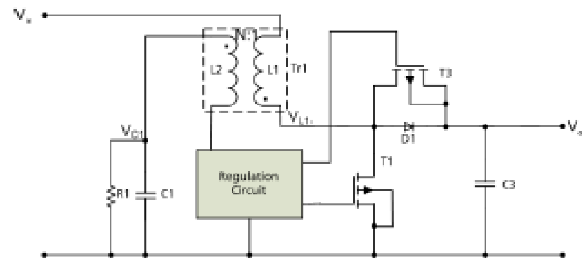


Figure 1: Self-oscillating dc-dc converter with 100 mV start-up voltage

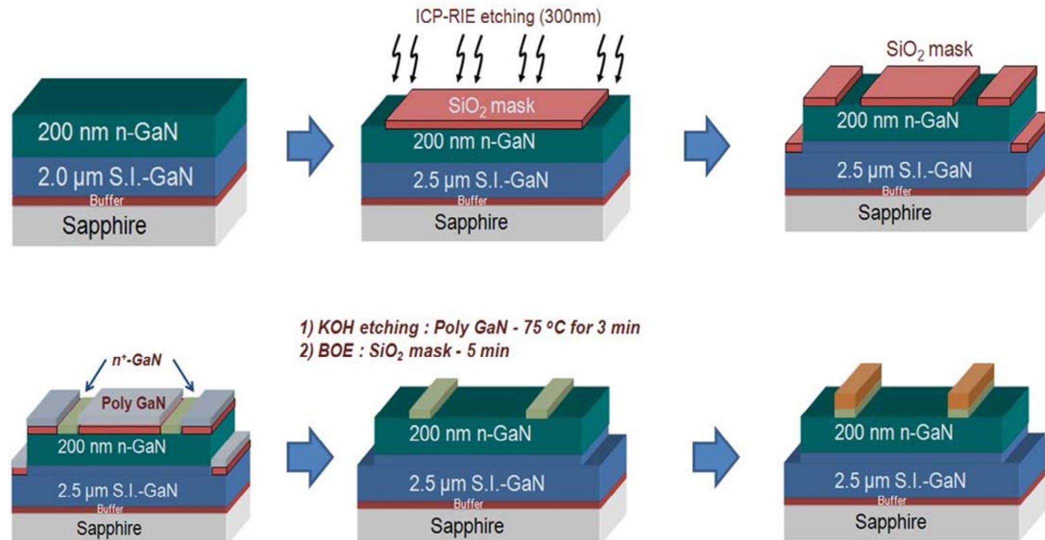
Presenters biography: Dipl.-Ing. Peter Spies studied Electrical Engineering at the University of Erlangen / Germany and graduated with a Dipl.-Ing. degree in 1997. Since 1998, he is with the Fraunhofer IIS, power efficient systems department. He was working on the field of multistandard frontends and system simulations for communication applications. Since 2001 he is group manager of the technologies for terminal devices group where he is doing research and design of integrated circuits, systems and software on the field of power and battery management, energy transmission and energy harvesting. He has several publications and holds several patents on that topic. Other areas of his work are sensor signal processing and interface technologies like wireless transceivers or transponders.

Abstract 2.5 – Oral Presentation

GaN-based power converters with integrated passive components

Patrick Lyle Chapman
University of Illinois at Urbana-Champaign, USA

Abstract:
Researchers in power electronics have been investigating miniaturization of power converters for many years now, with substantial progress toward viable converters completely on chip. One of the major challenges for converters on chip is the necessity of passive components that are both planar and small in size. Inductors, in particular, are more fundamentally three-dimensional devices so when confined to a plane, can occupy a disproportionate space. As such, power converters on silicon are at a disadvantage when trying to compete with discrete power converters on efficiency even if better power density can be obtained.
Since passive components are a significant issue, it makes sense to pursue better passive components as well as strive for high-frequency designs that can address directly the size of passive components. One potential way to drive the frequency higher is to consider compound semiconductors such as gallium nitride (GaN). GaN-based semiconductor devices have been used in optics and microwave amplifiers, and have some properties that may give them advantages over silicon or even other compound semiconductors like silicon carbide.
Our research has been to develop GaN-based transistors, such as high-electron-mobility transistors (HEMTS), that are now being tested and continuously improved toward higher current and frequency. We have also been working on hybrid inductor-capacitor devices that may aid in conserving footprint such that when combined with fast-switching GaN devices, may be successful in realizing efficient, fully-integrated converters on chip. Our presentation will cover our recent work in these respects.



Chip Embedding Technologies for Power Applications

Thomas Loeher and Andreas Ostmann
Fraunhofer Institute, Germany

Abstract: The presentation will give an overview of state of the art technologies for interconnection of power devices available at Fraunhofer IZM. Recent improvements and ongoing developments, such as double sided cooling and advances in die and wire bonding, will briefly be discussed.
Over the past six years technologies for the embedding of chips into build up layers of printed circuit boards, have been developed in various EU funded projects. These technologies are presently explored for the embedding of power components. The basic technologies and development progress will be presented.
An outlook for promising future enabling technology is the low temperature die bond interconnection using nano-structured surfaces.

Biography: Thomas Loeher, studied physics at University Göttingen and Technical University of Berlin, diploma in surface physics in 1992. In 1995 he was awarded Ph.D. from Freie Universität Berlin. From 1996 to 1999 he held a post-doc position at the University of Tokyo. He joined TU Berlin in 2002. His activities focus around embedding technologies in flexible (EU Project SHIFT) and stretchable materials (EU Project STELLA).

Session 3: Open Forum Discussion – Power Supply on Chip Vs Power Supply in Package

Monday, September 22nd, 2008 – 17.00 – 18.30

Chairs: Francesco Carobolante, Jeff Shepard, Cian Ó Mathúna, Joe O'Callaghan

PwrSoC and PwrSiP offer various levels of freedom and constraints, but complexity and cost as well as thermal and EMC issues are formidable challenges. This open-forum discussion will discuss if true "Power Supply on a Chip" is ever going to succeed or whether the constraints of the PwrSoC concept are so great that "System in Package" is the only solution. Forum speakers will provide brief opening statements for discussion by the workshop participants.

PWR SoC 08 Tyndall National Institute

Session 4: Integrated Passives –A) Magnetics and B) Capacitors

Tuesday, September 23rd, 2008 – 8.30 – 12.20

Chairs: Saibal Roy, Terence O'Donnell, Fred Roozeboom, Charles Sullivan, Masahiro Yamaguchi

Inductors and capacitors are key elements for any DC-DC converter. For power supply on chip, these passive components require novel and improved materials and integration techniques. In particular, multiMHz, soft magnetic materials and high dielectric constant (K) materials are needed to be deposited in a CMOS-compatible technique.
The issues to be addressed in this session include:

- Magnetic and capacitor integration - opportunities and challenges.
- Multi-MHz magnetics - thin film magnetics versus sintered ferrite vs. air-core.
- Silicon compatible capacitor materials and technologies.
- Material compatibility issues for integration of passives on top of active silicon.

4-A) Magnetics:

Time	Speakers	Affiliation	Country	Title of the talk
08:30-08:55	Shan X Wang	Stanford University	USA	Embedded Integrated Inductors with a Single Layer Magnetic Core: Performance Gains and Trade-offs
08:55-09:20	Charles R. Sullivan	Dartmouth College	USA	Losses in laminated thin-film magnetic materials considering displacement current
09:20-09:45	Masahiro Yamaguchi	Tohoku University	Japan	Ferromagnetic integrated inductor/noise suppressor
09:45-10:10	Terence O'Donnell	Tyndall National Institute	Ireland	High efficiency inductors on silicon
10:10-10:40	Poster Presentation, Coffee/Tea Break			

4-B) Capacitors:

Time	Speakers	Affiliation	Country	Title of the talk
10:40-11:05	Magali Brunet	LAAS CNRS	France	3D capacitors on silicon with high density pores network and ZrO_2 dielectric films deposited by MOCVD
11:05-11:30	Gordon Grivna, Sudhama Shastri, Yujing Wu, Will Z. Cai	On Semiconductor	USA	A Low Series Resistance, High Density Trench Capacitor for High-Frequency Applications
11:30-11:55	Charles Divita	Gennum Corporation	Canada	Applications, Processing and Integration Options for High Dielectric Constant, Multi-Layer Thin-Film Barium StrontiumTitanate (BST) Capacitors
11:55-12:20	Fred Roozeboom et al	NXP Semiconductors	Netherlands	Ultrahigh-density (> 0.4 µF/mm2) trench capacitors in Silicon
12:20-13:30	Clarion Hotel, Lunch			

Abstract 4.1 – Oral Presentation

Embedded Integrated Inductors with a Single Layer Magnetic Core: Performance Gains and Trade-offs

Shan X. Wang, Dok Won Lee, and Liangliang Li
Dept. of Materials Science and Engineering, Dept. of Electrical Engineering, Stanford University, Stanford, California 94305, USA email: sxwang@stanford.edu.

Because embedded inductors are placed directly on Si wafers or in packages for integrated circuits, they truly enable the realization of the integrated electronics such as system-on-a-chip (SoC) and system-in-package (SiP). Integrated solenoid inductors with magnetic core were fabricated and analyzed [1,2]. An inductance above 70 nH was achieved while keeping the coil resistance below 1 Ω and the device area below 1 mm^2 using a solenoid design with a single magnetic CoTaZr layer (Figure 1). The inductance of the magnetic inductor was more than 30 times that of the air core inductor of the identical geometry, and the quality factor of the magnetic inductor was > 5. Novel inductor designs and the scalability were also examined, and an inductance density higher than 200 nH/mm^2 was obtained. The measured device properties and engineering trade-offs were well explained by analytical models we developed.

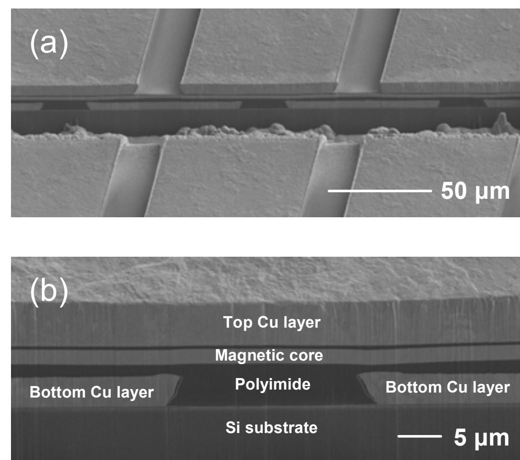


Fig. 1: FIB cross-section images of the standard Cu solenoid inductor with CoTaZr magnetic core, deposited on planarized polyimide.

We have also designed and fabricated both single-coil and parallel-coil magnetic integrated inductors with extremely small resistances (~10 mΩ) and high quality factors (>23) on an 8-inch round printed circuit board (PCB) substrate for microprocessor power delivery applications [3]. The DC resistances of these inductors are less than 12 mΩ. Soft magnetic material CoFeHfO was successfully integrated into the inductor fabrication to increase the inductance. The quality factors (Q) are more than 80 in a frequency range of 1.5 to 2 GHz for air-core inductors, and more than 23 in a range of 200 to 300 MHz for magnetic inductors. The net inductance improvement of the magnetic inductor over air-core inductor is about 12%, which could be further enhanced with a thicker magnetic core, according to our theoretic calculation. We also characterized the permeability spectra of CoFeHfO material on the PCB substrate, simulated the high-frequency performance of the magnetic integrated inductor by HFSS, and reached a good agreement with the experimental data. The experimental and simulation results of the magnetic inductors as compared to those of the air-core inductors point out the future direction to further optimize magnetic integrated inductors.

[1] D. Lee, L. Li and S. X. Wang, "Embedded Inductors", book chapter to appear in Materials for Advanced Packaging, Daniel Lu, CP Wong, Eds., Springer, 2008.
[2] D. W. Lee, K.-P. Hwang and S. X. Wang, "Fabrication and analysis of high-performance integrated solenoid inductor with magnetic core (invited)," IEEE Trans. Mag., in press, 2008.
[3]L. Li, D. Lee, K. P. Hwang, et al., "Small resistance and high Q magnetic integrated inductors on PCB," submitted to IEEE Transactions on Advanced Packaging, 2008.

Short Biography of the speaker:

Dr. Wang currently serves as the director of the Stanford Center for Magnetic Nanotechnology and is a full professor in the Department of Materials Science & Engineering and jointly in the Department of Electrical Engineering at Stanford University. He is also with the Geballe Laboratory for Advanced Materials, and is affiliated with Stanford Bio-X Program. His current research interests lie in magnetic nanotechnologies and information storage in general and include magnetic biochips, magnetic nanoparticles, nano-patterning, spin electronic materials, magnetic inductive heads, as well as magnetic integrated inductors and transformers. He has published over 150 papers, and holds 17 patents (issued and pending) on these subjects. He and Alex Taratorin published a book titled "Magnetic Information Storage Technology" through Academic Press. Dr. Wang contributed two book chapters on magnetic biochip and embedded inductors, respectively, and gave more than 50 invited presentations in major scientific conferences and meetings. He received the B.S. degree in physics from the University of Science and Technology of China in 1986, the M.S. in physics from Iowa State University in 1988, and the Ph.D. in electrical and computer engineering from the Carnegie Mellon University (CMU) at Pittsburgh in 1993.

Abstract 4.2 – Oral Presentation

Losses in laminated thin-film magnetic materials considering displacement current

Charles R. Sullivan and Di Yao
Thayer School of Engineering, Dartmouth College, Hanover, NH, USA

Thin-film magnetic materials are attractive for making high-power-density transformers and inductors on-chip or co-packaged with a power system-on-a-chip. They can have lower hysteresis loss and higher saturation flux density than ferrites. However, they usually have lower resistivity, which can lead to high eddy-current loss. The geometry of a thin film reduces eddy currents for flux traveling in the plane of the film, but the loss can still be problematic, and magnetic films are often laminated with dielectric material separating each layer in order to reduce eddy-current losses. Standard analysis of loss in these multi-layer films assumes that the dielectric layers block any large-scale eddy currents, and that eddy currents only circulate within individual layers. However, with thin films at high frequencies, the capacitance across the dielectric layer becomes important and displacement currents flowing through the dielectric can become significant. We have studied and modeled these losses.

Finite-element simulations were used to determine the losses including displacement current effects, based on a layer-by-layer model for small numbers of layers and a homogenized anisotropic parameter model for approximating a large numbers of layers. Simulation results were combined with analytical calculation of asymptotic behavior to construct a closed-form expression to approximate loss as a function of geometry and material properties. Simulations conducted over a wide range of parameter values show that the model is valid for nearly all practical configurations.

The results show that dielectric layers can be highly effective in reducing eddy-current losses in thin film materials, but that the losses in many practical cases are still several orders of magnitude higher than would be predicted without considering dielectric losses. Predicted loss in a sample of multilayer Co-Zr-O/Zr-O shows good agreement with experimental measurements.

Biography:

Charles R. Sullivan is presently Associate Professor at the Thayer School of Engineering, Dartmouth College, Hanover, NH. He received a B.S. in electrical engineering with highest honors from Princeton University in 1987 and a Ph.D. in electrical engineering from the University of California, Berkeley in 1996. Between these degrees, he worked for Lutron Electronics designing electronic ballasts. He has over 90 peer-reviewed conference and journal publications and 15 US patents. His research includes work on design optimization of magnetics for high-frequency power conversion, thin-film magnetic materials and devices for power applications, topologies and components for microprocessor power delivery, and electromagnetic modeling of capacitors. He is the recipient of a National Science Foundation CAREER award and a Power Electronics Society Prize Paper Award. He serves as Associate Editor for the Transactions on Power Electronics and Awards Chair for the Power Electronics Devices and Components Committee of IAS.

Abstract 4.3 – Oral Presentation

Ferromagnetic integrated inductor/noise suppressor

Masahiro Yamaguchi
Department of Electrical and Communication Engineering, Tohoku University; 6-6-05 Aoba, Aramaki, Aoba-ku, Sendai 890-8579, Japan; E-mail: yamaguti@ecei.tohoku.ac.jp, URL: http://www.itmag.ecei.tohoku.ac.jp/

Abstract: Development of miniaturized and fast-response electronic devices has been accelerated by the System-in-Package (SiP) technology. Advanced three dimensional packaging technology including the stacked multi-chip package and Package-on-Package (PoP) are also growing because of a further demand on the integration of new functions for example to the digital household appliances and cell phone systems. Integrated power solutions are therefore necessary.

Ferromagnetic thin/thick film is a key material to realize low-loss and miniaturized integrated inductive components for DC-DC converter. It is necessary for the magnetic material for an integrated inductor to have high saturation moment and low coercive force, as well as microfabrication process compatibility and thermal/stress toughness. The L.L.G. equation reminds us the basic dynamics of magnetic moment as $\mu_i = M_s/H_k$, $f_{fmr} = (\gamma/2\pi) x(M_sH_k/\mu_0)^{1/2}$ and $\mu_i f_{fmr}$=const for uniaxial film, showing that a magnetic film with high M_s and low H_k is essential to realize a good power inductor for MHz-range operation.

A broad bandwidth complex permeameter up to 9GHz was developed and applied for evaluating amorphous alloys, granular and composite thin films to discuss this idea [1].

Utilizing the real part of complex permeability, ferromagnetic RF integrated inductor was developed and have drawn attention of microwave engineers because of future possibility of further miniaturization and high-Q in monolithic microwave integrated circuit (MMIC). A slit work on the magnetic film [2], [3] is useful to align magnetic moment to a certain direction based on shape anisotropy, as well as to reduce the in-plane eddy current losses. Performance of Q=20 at 1-2 GHz has been demonstrated for ferromagnetic spiral inductors.

Once a power supply is enclosed in a package or on a chip, the surrounding electronics may be subjected to electromagnetic noise from the power supply with the frequency range up to/over 1 GHz. Then the magnetic film can take a role to shield the electromagnetic field in an integrated form. The imaginary part permeability and the Ferromagnetic Resonance (FMR) losses are also useful to dissipate the high frequency noise power into heat. The noise suppression sheet (NSS) has been used popularly and its measurement standard has just been established in May 2006 by IEC (International Electrotechnical Commission.) Thin film type NSS [4] has been studied and exhibited insersion loss 47dB on coplanar transmission line at 10GHz, using a CoPdAlO granular film [5].

Suppose the power supply module of a cryptographic chip is subjected to the powerful side channel attacks of Differential Power Analysis (DPA) and Differential Electromagmetic Analysis (DEMA). Then the secret key may be stolen [6]. Therefore the thin film NSS is also useful to hide instantaneous circuit operation of an LSI chip.

In conclusion, ferromagnetic films have a number of crucial roles in DC-DC converter in an integrated form in terms of increasing power density, settling electromagnetic environment and improving the information security.

References:

[1] M. Yamaguchi, Y. Miyazawa, K. Kaminishi and K.I. Arai, “A New 1 MHz-9 GHz Thin-Film Permeameter Using a Side-Open TEM Cell and a Planar Shielded-Loop Coil,” Trans. Magnetics Society of Japan, **3**, 137-140 (2003).

[2] M. Yamaguchi, K. Suezawa, M. Baba, K. I. Arai, Y. Shimada, S. Tanabe, and K. Itoh, “Application of Bi-Directional Thin-Film Micro Wire Array to RF Integrated Spiral Inductors,” IEEE Transactions on Magnetics, **36**, 3514-3517 (2000).
[3] Masahiro Yamaguchi, Keiju Yamada, Ki Hyeon Kim, "Slit Design Consideration on the Ferromagnetic RF Integrated Inductor," IEEE Transactions on Magnetics, **42**, 3341-3343 (2006).
[4] Shigeyoshi Yoshida, Hiroshi Ono, Shinsuke Ando, Fumishiro Tsuda, Tetsuo Ito, Yutaka Shimada, Masahiro Yamaguchi, Ken-Ichi Arai, Shigehiro Ohnuma, Tsuyoshi Masumoto, “High-Frequency Noise Suppression in Downsized Circuits Using Magnetic Granular Films,” IEEE Trans. Magn., **37**, 2401-2403 (2001).
[5] Ki Hyeon Kim, Shigehro Ohnuma, Masahiro Yamaguchi, “RF Integrated Noise Suppressor Using Soft Magnetic films,” IEEE Transactions on Magnetics, **40**, 2838-2840 (2004).
[6] Paul Kocher, Joshua Jaffe, Benjamin Jun, "Differential Power Analysis", CRYPTO'99, pp.388-397, 1999.

Speaker Biography: Masahiro Yamaguchi

March 1984	Ph. D, Department of Electrical and Communication Engineering, Tohoku University
April 1984	Research Associate, Department of Electrical and Communication Engineering, Tohoku University
July 1991	Associate Professor, Research Institute of Electrical Communication, Tohoku University
Oct-Dec 1995	Visiting Associate Professor, Wisconsin Center for Applied Microelectronics, University of Wisconsin-Madison, The United States.
April 2003	Professor, Department of Electrical and Communication Engineering, Tohoku University

He is interested in permeable application of ferromagnetic thin films for integrated inductors and electromagnetic noise suppressors.

He organizes annual International Workshop on the high frequency micromagnetic devices and materials, MMDM, since 2002. He is currently the Editor-in-Chief of the Magnetics Society of Japan, and a Board Member of Japan Institute of Electronics Packaging.

Abstract 4.4 – Oral Presentation

High efficiency inductors on silicon

T. O'Donnell[1], N. Wang[1], R. Meere[1], F. Rhen[1], S. Roy[1], Ray Foley[2], Jason Hannon[2] C. O'Mathuna[1]

[1]Tyndall National Institute,
Lee Maltings, Prospect Row
Cork, Ireland.
[2]Power Electronics Research Lab, University College Cork,
Cork, Ireland. Email: terence.odonnell@tyndall.ie

Abstract: This presentation presents the design and measured results for micro-fabricated inductors suitable for use in high frequency (> 10 MHz), low power (1 –2 W) dc-dc converters. The micro-inductor structure consists of a racetrack shaped copper coil, surrounded by layers of magnetic material. The magnetic core consists of electro-deposited layers of anisotropic 45/55 Nickel Iron alloy. One of the most important goals for micro-inductor design is the minimisation of the overall loss in the inductor when used in a dc-dc converter. Thus the inductor design optimisation has focused on maximizing inductor efficiency for a given converter specification. It can be seen from the design optimisation that there exista a trade-off between inductor efficiency and footprint area.
Micro-inductors in the range of 100 nH to 300 nH have been fabricated and tested. The small signal measurements show a relatively flat inductance profile, with a 10% drop in inductance at 30 MHz. Inductance vs. dc bias current measurements show less than 15% decrease in inductance at 500 mA current. The performances of the micro-inductors have also been compared to a conventional wire-wound inductor in a 20 MHz dc-dc converter. The converter efficiency is shown to be approximately 4% lower when the micro-inductor is used compared to when the wire-wound inductor is used. The peak efficiency of the micro-inductor in the converter is estimated to be approximately 93%.

Speaker biography: Terence O'Donnell received his BE in electrical engineering from University College, Dublin in 1991. In 1996 he received his Ph.D degree from University College Dublin for research in the area of Finite Element Analysis of magnetic field problems. He is presently a Senior research officer based in the Tyndall National Institute in Cork, where he is currently leading the research activity on integrated magnetics. He has worked on numerous research projects relating to design, modelling and fabrication of planar magnetics for power conversion and data communications, integrated RF inductors, magnetic field sensors, magnetics for remote inductive powering and electromagnetic generators for the harvesting of energy from ambient vibrations.
Current research interests include the design, modelling and fabrication of integrated magnetic components. He has a particular focus on the integration of magnetic components onto Silicon for power conversion applications..

Abstract 4.5 – Oral Presentation

3D capacitors on silicon with high density pores network and ZrO_2 dielectric films deposited by MOCVD

Magali Brunet[a], Gérald Leclerc[a], Emmanuel Scheid[a], Jean-Louis Sanchez[a]
Karolina Galicka-Fau[b], Michel Andrieux[b], Corinne Legros[b], Isabelle Gallet[b], Michaële Herbst[b]
Pascal Kleimann[c].

[a] Université de Toulouse, Laboratoire d'Analyse et d'Architecture des Systèmes, LAAS, CNRS UPR 8001, 7 av. du Colonel Roche, F-31077 Toulouse Cedex, France.
[b] Université de Paris Sud 11, Laboratoire d'Etude des Matériaux Hors Equilibre, LEMHE, CNRS UMR 8647, Bâtiment 410, F-91405 Orsay Cedex, France.
[c] Université Lyon 1, Institut des Nanotechnologies de Lyon, INL, CNRS UMR 5270, 8 rue Ampère, F-69622, Villeurbanne, France.

The presented work deals with high-density integrated capacitors for output filters in future micro DC-DC converters. In low power portable applications, integrated passive components are necessary to produce miniaturized systems. When talking about integrated capacitors, the actual solutions on silicon (MOS or MIM) are not able to produce the capacitance values required for 1W DC-DC converter: more than 1µF/mm² at 10 MHz. To increase the capacitance density, the first approach is to work on the capacitor geometry: reduced dielectric thickness and maximised electrodes area. The second approach concerns the use of a high-k dielectric. In the presented work, we are combining these two approaches.

3D capacitors structures were realised in a high conductivity silicon substrate with deep cavities network etched by two methods: DRIE and electrochemical etching. Very high capacitance density can be reached by increasing the pores density and the pores aspect ratio (depth/width). Going down to submicronic pitches with very high aspect ratios pores is of the greatest interest. It was shown that the electrochemical etching technique [1] could reach these objectives: pores with aspect ratios of 133 were produced.

In a second part, the SiO_2/Si_3N_4 standard dielectric stack was compared to ZrO_2 (k =25- 40). The ZrO_2 films (about 100 nm) were deposited by liquid injection MOCVD from $Zr_2(O^iPr)_6(thd)_2$. The deposition parameters were optimised in order to obtain at the same time uniform films (without cracks) and good stoichiometry without carbon contaminants. The films were constituted of a mixture of tetragonal and monoclinic phases. The deposition parameters were varied in order to promote the tetragonal phase (permittivity reported around 40 [2]). In parallel, the 3D coverage of ZrO_2 film was observed in pores with SEM. It reveals two deposition regimes: a surface reaction controlled regime for low aspect ratios (depth/width) and a diffusion controlled regime for high aspect ratios (> 2). Electrical characterization of the ZrO_2 films on planar MIS structures allowed an estimation of the permittivity (24-27).

These dielectric properties combined with 3D deposition will allow the realisation of very high-density capacitors.

[1] P. Kleimann et al. App. Phys. Lett., 2005.
[2] Zhao et al. Phys Rev B, vol 65, 075105, 2001.

Biography :

Magali Brunet obtained her PhD in Microelectronics Engineering in 2003 from University College Cork, Ireland. Since 2005, she is a research scientist at Laboratory of Analysis and Architecture of Systems (LAAS – CNRS) in the group Integration of Power Management Systems. Her research is focused on integrated passive components (microinductors, microtransformers, microcapacitors) for power electronics. She is looking in particular at the fabrication techniques and the integration of new materials.

Abstract 4.6 – Oral Presentation

A LOW SERIES RESISTANCE, HIGH DENSITY TRENCH CAPACITOR FOR HIGH-FREQENCY APPLICATIONS

Gordon Grivna, Sudhama Shastri, Yujing Wu, Will Z. Cai
On Semiconductor, USA

Abstract:
Integrating high-Q capacitors with transistors, inductors and resistors on the same chip is a hot research field for achieving monolithic microwave integrated circuits, including radio-frequency (RF) signal generation and filtering [1-3]. Furthermore, the integration of passive or active RF circuitry on VLSI chips is increasingly common, and leads to the creation of more complex systems-on-chip. In particular, high-density, high-Q capacitors are desired for supply-bypass and decoupling applications. In a traditional planar capacitor, there is the well-known trade-off between capacitance density and leakage current. In order to shrink the size of capacitor without adversely affecting its leakage characteristics, three-dimensional capacitors have been implemented [4, 5] in which a dielectric material is deposited along the vertical sidewall of a trench or pillar, as well as on the top and bottom flat regions. We have fabricated a novel, cost effective, Si VLSI-compatible polysilicon-insulator-polysilicon (PIP) trench capacitor with a specific capacitance of 8-30 fF/μm^2 [6], much higher than the 1.5 fF/μm^2 for a traditional planar capacitor. The process integration, electrical characterization, SPICE (compact) modeling, and reliability evaluation will be reported.

Biography: Gordon Grivna is Director of Advanced Silicon Integration for Corporate R&D of ON Semiconductor with 27 years of processing and integration experience. He can be reached at: Gordy.Grivna@onsemi.com, 602-244-7458.

Sudhama Shastri has spent almost 20 years in the semiconductor industry and is currently responsible for design and product development at California Micro Devices. His previous roles included Director of High-Frequency Technology Development at ON Semiconductor and Senior Principal Engineer at Digital DNA Labs in Motorola. He received a BTech degree at the Indian Institute of Technology and MS and PhD degrees at the University of Texas. He serves on the board of the Arizona Nanotechnology Cluster, on the Technical Program Committee for NSTI's annual Nanotech Symposium. He is a reviewer for IEEE journals, and has over 50 publications and 5 issued patents. He can be reached at sudhamas@cmd.com, 480-966-0033.

Yujing Wu is a device development engineer for Corporate R&D of ON Semiconductor. She can be reached at: Yujing.wu@onsemi.com.

Dr. Will Cai is Director of engineering of EngMax, a firm specializing in semiconductor process/device simulations of 0.13um CMOS and exotic III-V technologies. Dr. Cai has previously served in technical and managerial positions at several leading companies in the semiconductor industry. He is the editor of two books and has published over 45 papers in technical journals and conference proceedings. He is a frequent reviewer for the IEEE and the American Vacuum Society. He received Jazz Semi's Maestro Award in 2006 and the Excellence of Services Award from the Transworld Research Network Publisher in 2003.
He has been listed in Marquis Who's Who in America, and Who's Who in the World since 2002.

Abstract 4.7 – Oral Presentation

Applications, Processing and Integration Options for High Dielectric Constant Multi-Layer Thin-Film Barium Strontium Titanate (BST) Capacitors

Charles Divita
Gennum Corporation, Canada

Abstract:
To date integration of capacitors has been restricted to low capacitance values limited primarily by the materials and technologies employed. The combination of multi-layered thin film technology along with high K dielectric Barium Strontium Titanate (BST) enables capacitance densities of 100nF/mm². Applications demanding high quality low inductance decoupling and/or significant miniaturization are ideal candidates for this technology. Integration with other passives devices (resistors and inductors) has been demonstrated and options for integration with active devices are identified.

Gennum Background:
Gennum Corporation (TSX: GND) designs innovative semiconductor solutions and intellectual property (IP) cores for the world's most advanced consumer connectivity, video broadcast and data communications products. Leveraging the company's proven optical, analog and mixed-signal products and IP, Gennum enables multimedia and data communications products to send and receive information without compromising the signal integrity.

Speaker Biography:
Charles Divita has held various positions including design, management and technology development with over 20 years experience in microelectronics. Presently responsible for business development and project management for BST technology at Gennum Corporation.

Ultrahigh-density (> 0.4 μF/mm²) trench capacitors in silicon

F. Roozeboom[1,2], W. Dekkers[1], K.B. Jinesh[1], W. Besling[1], Y. Lamy[1],
J.H. Klootwijk[3], M.A. Verheijen[4], H.-D. Kim[4] and D. Blin[5]

[1] NXP-TSMC Research Center, High Tech Campus 4, 5656 AE Eindhoven, The Netherlands,
[2] Eindhoven University of Technology, Dept. Technical Physics, 5600 MB Eindhoven, The Netherlands,
[3] Philips Research, High Tech Campus, 5656 AE Eindhoven, The Netherlands,
[4] Jusung Engineering, Gyunggi-Do, Korea 464-890, [5] Jusung Engineering Europe, 38920 Crolles, France

One trend in advanced micro- and nanoelectronics with a small form factor described in the latest ITRS roadmap is the increasing use of the 3rd dimension. This holds not only for mainstream System-on-Chip (*SOC*) technology. Even more it holds for 3D heterogeneous and homogeneous System-in-Package (*SiP*) integration accomplished by stacking dies and wafers containing through-wafer interconnects (vias) and for passive integration components such as trench capacitors.
NXP recently launched its PICS (*Passive Integration Connecting Substrate*) technology for application in highly integrated cellular RF transceiver modules. Here, back-end Si processing is used to integrate passives (high-Q inductors, resistors, and capacitors) [1]. The Si dies thus made can serve as a platform for heterogeneous integration with active component dies, MEMS dies, etc. Key in this platform are, in particular, high-density (~25 nF/mm²) MOS 'trench' capacitors for RF-decoupling and filtering.
In this paper we describe the growth of 3D 'trench' capacitors in Si with a world record ultrahigh capacitance density of ≥ 400 nF/mm² and breakdown voltage > 6 V using thermal ALD of multiple MIM (Metal-Insulation-Metal) layer stacks of 'high-k' dielectrics (Al_2O_3) and conductive layers (TiN). The stack shown in Fig. 1a contains a first dielectric layer of 5 nm thermally grown SiO_2 with a stack of $TiN/Al_2O_3/TiN/Al_2O_3/TiN$ on top to complete a triple MIM capacitor. TiN layers were grown at 400 °C from $TiCl_4$ and NH_3 vapor dosing and the Al_2O_3 layers were grown at 380 °C from trimethyl aluminum (TMA) and O_3, both in a Jusung Eureka™ reactor while avoiding the oxidation of the TiN layers. Precursor pulse/purge ratios were optimized for optimum step coverage across macropores of 30 μm depth and ~ 1.5 μm width. The mask design used allowed the simultaneous formation of planar and trench capacitors and the subsequent electrical testing of the individual capacitors as well as the total capacitor stack. Part of the wafers were annealed in O_3 (5 mins. at 400 °C) after each Al_2O_3 deposition step to suppress the dielectric leakage and to improve breakdown voltage. The final results are shown in Figs. 1b and 1c.
The ultrahigh densities reached with this concept opens up new application fields such as DC-DC conversion, integrated in silicon. With future 'high-k' dielectrics containing, e.g. rare earth oxides or Sr-Ti-O, the barrier of 1 μF/mm² capacitance densities may soon be taken.

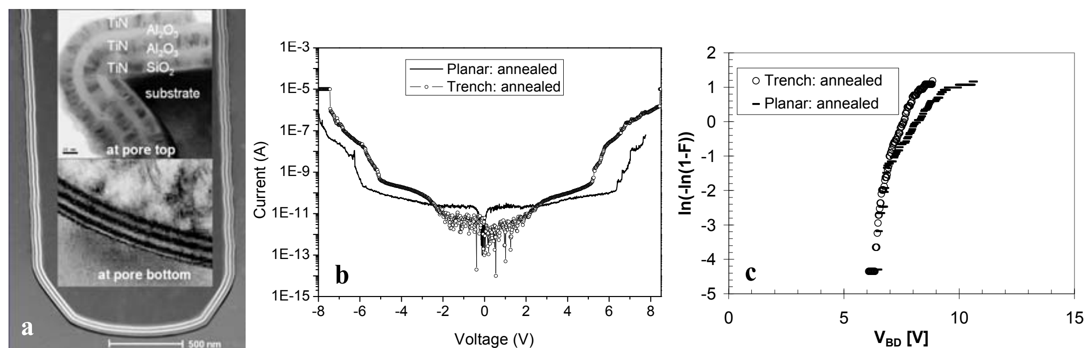


Fig. 1. Triple MIM capacitor: (a) Bright-field TEM image and STEM-HAADF images (insets); b) I-V curves and c) Weibull-plot for electrical breakdown voltage for planar and trench capacitors after annealing in O_3.

[1] F. Roozeboom et al., Thin Solid Films **504,** 391 (2006).

[1] F. Roozeboom et al., Thin Solid Films **504,** 391 (2006).

Speaker Biography: Prof. Dr. Fred Roozeboom, born Sept. 9, 1952, is a Research Fellow at NXP Semiconductors Research (until Sept. 2006: Philips Research) in Eindhoven, The Netherlands. He received his MSc in chemistry (cum laude) from the University Utrecht, The Netherlands in 1976, and his PhD in chemical engineering in 1980 at Twente University (Enschede, The Netherlands) on topics in catalysis. From 1980-1983 he worked on zeolite catalysis with Exxon R&D Labs in Baton Rouge, USA (1980-1982) and with Exxon Chemicals in Rotterdam (1983).

Late 1983 he joined Philips Research in Eindhoven, where since 1997 he leads a team working on passive and hetero-integration, in particular on viahole technology and 3D integration for application in System-in-Package products and on high-value passives in silicon for application in wireless communication, power management and digital signal processing. For part of this work he received the Bronze Award of the 'NXP Invention of the Year 2007'. He is also a technical advisor to the EMC3D consortium (www.emc3d.org).

His earlier work at Philips encompassed MOCVD of III-V semiconductor lasers (1983-1988), IC metallization materials deposition and processing (1988-1990) and on bulk ferrite and thin-film soft-magnetic materials for magnetic recording (1990-1996). In 1996 he has been working on MBE of ultrathin magnetic and "switchable mirror" hydride multilayers.

In 1995 he was the director of a NATO Advanced Study Institute on Rapid Thermal and Integrated Processing. He has authored or co-authored ~ 130 journal and conference publications, holds several patents, and is the editor or co-editor of seventeen conference books on semiconductor processing.

He serves as a member-at-large of the Electronics and Photonics Division of the Electrochemical Society, as a member of the ENIAC advisory committee to the European Commission (subcommittee "Beyond CMOS") and as a member of the IMAPS Benelux committee. He also served as a Meeting Chair of the Materials Research Society (MRS) Fall 2003 Meeting and as a member of the MRS Strategic Program Development Subcommittee. Since 2007 he is also a part-time professor at the Department of Technical Physics of the University of Technology in Eindhoven, The Netherlands, in the group Plasma and Material Processing.

Session 5: Converter topologies and control systems for PwrSoC

Tuesday, September 23rd, 2008 – 13.30 – 16.30

Chairs: Dragan Maksimovic, Seth Sanders, Dave Perreault

This session addresses power train circuits and controller design for on-chip and other power supplies targeting miniaturization or integration with loads. The session will present the latest advances in converter circuit topologies, including high-frequency, multi-phase or multi-level configurations, resonant power converters operating at RF frequencies, switched-capacitor circuits, topologies that enable ultra-high density miniaturization etc., as well as control systems enabling efficient operation at high frequencies. Light load efficiency issues will also be considered in the context of battery performance in mobile applications.

Time	Speakers	Affiliation	Country	Title of the talk
13:30-13:55	Baoxing Chen	Analog Devices	USA	Fully integrated isolated dc-dc converter and half bridge gate driver with integral power supply
13:55-14:20	Dave Perreault	MIT	USA	Architectures, Topologies and Design Methods for Miniaturized VHF Power Converters
14:20-14:45	Elad Alon	UC Berkeley	USA	Supply Impedance and Voltage Conversion Requirements for CMOS Digital ICs
14:45-15:15	Poster Presentation, Coffee/Tea Break			
15:15-15:40	Eduard Alarcón	UPC Barcelona	Spain	Optimization and implementation of a multi-level buck converter for standard CMOS on-chip integration
15:40-16:05	Seth R. Sanders	UC Berkeley	USA	What about switched capacitor converters?
16:05-16:30	José A. Cobos	UPM Madrid	Spain	Fast dynamics with non linear control: merits and limitations
18:30	Banquet: Bus to Blarney from Clarion Hotel			
19:00-23:00	Workshop Banquet			
23:00	Bus to Cork			

Abstract 5.1 – Oral Presentation

Fully Integrated Isolated dc-dc Converter and Half Bridge Gate Driver with Integral Power Supply

Baoxing Chen
Analog Devices, Inc. USA

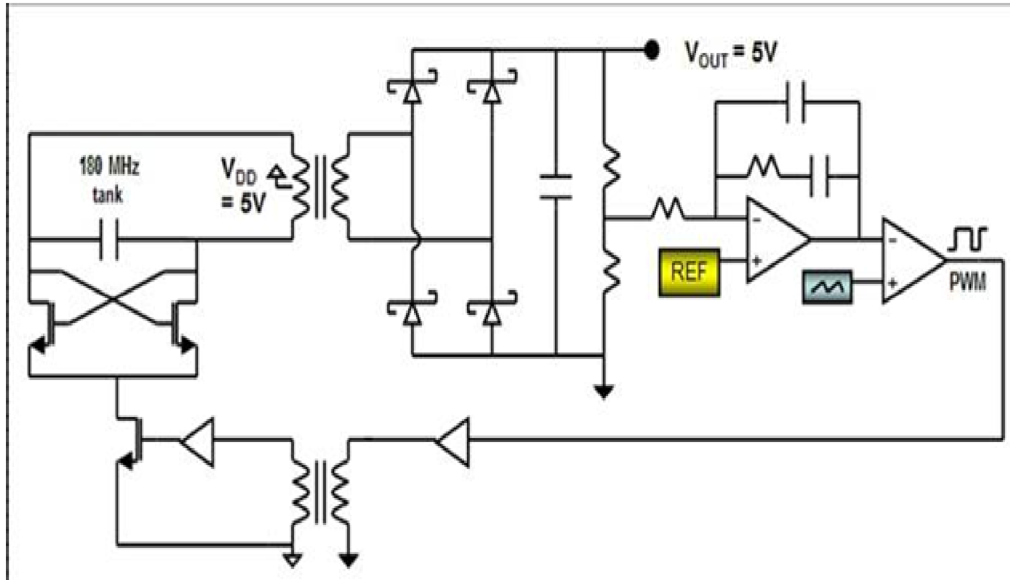
The integration of DC-DC converters invloves integration of transformer switches, rectification diodes, and passive components such as inductors and capacitors. The passive components can be scaled down by increasing switching frequnecy. However, the regulation becomes difficult once the switching frequency increases. We can solve this difficulty by separating energy converion from energy regulation. In essence, we optimise power transfer with self-oscillating high frequency transformer driver while turning on/off the oscillator at a much lower frequency to regulate the power transfer.

The on-chip spiral inductors were used to build isolated transformers. The series resistance is minimized through the use of 6μm thick plated Au for both the primary and the secondary spirals. The 20μm or 30μm thick polyimide in between the primary and the secondary provides the needed HV isolation, up to 5KV. The additional 5μm thick polyimide under the bottom spiral helps to reduce substrate capacitance and substrate loss. The substrate loss is further reduced through careful designed patterned ground shield using underlying IC metal. The proximity effect and eddy current loss is less of concern for closed coupled inductors.

The architecture for the isolated DC-DC converter is shown in below figure. The two HV NMOS in a cross-coupled configuration provides the positive feedback to sustain the LC tank oscillation. The Schottky diodes were used as rectification devices at the secondary. These Schottky diodes would turn on and recover fast enough for a 300MHz rectification but maintain a good reverse breakdown voltage, especially useful for the rectification of voltage higher than 5V that an on-chip diode from standard NPN can not handle.

Because of the nature of multi-resonance for the transformer coupled oscillator, the size of the Switching components and Schottky diodes need to be sized such that the energy transfer won't get stuck at the low efficiency resonance mode, typically at higher frequency than that of high efficiency mode. Moreover, the diodes need to be sized so that they will stay in Schottky regions.

Signal and power isolation using microtransformers enabales the integration for other power components. Fully integrated half-bridge gate driver with integral high side power supply will be discussed.



Biography:
Baoxing is a Sr. Staff Engineer at Analog Devices, Inc. He received his Ph. D in Physics and MS in EE from U of Michigan in 1997. He pioneered the use of micro-transformers for transmitting signal and power across isolation barrier. Baoxing has published more than 20 papers and holds 7 US patents.

Abstract 5.2 – Oral Presentation

Architectures, Topologies and Design Methods for Miniaturized VHF Power Converters

David Perreault
Massachusetts Institute of Technology, USA

Abstract:

Electrical energy is the cornerstone of our technological infrastructure, and its use pervades our society. Advances in power electronics are becoming vital, both for addressing the growing energy challenges we face and for extending our control over the world around us. Challenges of particular importance include miniaturization and integration of power circuits. Likewise, advances in the performance of power electronics – including efficiency, control bandwidth, and operating range – are essential to reducing energy consumption and increasing functionality in myriad applications.

This talk describes ongoing research at MIT that seeks to address the challenges of miniaturization, integration, and performance of power electronics. System architectures, circuit topologies, and control methods will be introduced that facilitate dramatic increases in the switching frequencies of dc-dc converters (e.g., into the VHF range of 30-300 MHz). Higher frequencies are desirable because they reduce energy storage requirements, but necessitate circuit designs that either compensate for or utilize device parasitics. Converter topologies that meet these requirements and provide low voltage stress and fast transient response will be described. Likewise, key circuit building blocks and control methods will be discussed that enhance achievable performance in the VHF range. Design considerations for integrated power semiconductors and passive components in these architectures will also be addressed. Experimental results from power converters operating at frequencies of up to 110 MHz will be presented to illustrate these emerging technologies.

Speaker Biography:

David Perreault received the B.S. degree from Boston University and the S.M. and Ph.D. degrees from the Massachusetts Institute of Technology, all in Electrical Engineering. He is presently Associate Professor of Electrical Engineering and Computer Science at the Massachusetts Institute of Technology. His research interests include design, manufacturing, and control techniques for power electronic systems and components, and in their use in a wide range of applications.

Abstract 5.3 – Oral Presentation

Supply Impedance and Voltage Conversion Requirements for CMOS Digital ICs

Elad Alon
University of California, Berkeley

Abstract: CMOS chips have evolved to operate at steadily lower supply voltages and increasing power densities, leading to drastic reductions in the required impedance of the supply distribution network. For example, today's 1V, 100A microprocessors require a supply impedance of ~1mΩ, which is extremely challenging to achieve even at low frequencies. Thus, the impact of an integrated power converter on the impedance of the power distribution network is one of the key considerations in such a design. Indeed, one of the main motivations behind initial explorations of fully integrated DC-DC converters was the relaxed resistance required of the package and board-level power networks.

Since synchronous digital circuits must meet their cycle-time requirements under the worst-case conditions, the supply network must maintain not only low DC resistance, but low AC impedance as well. Thus, in the first part of this talk I will describe my previous work on a parallel, linear regulator whose goal is to reduce the AC supply impedance without negatively increasing the overall power dissipation of the chip. The key to achieving this goal lies in the realization that it is the minimum supply voltage that sets chips performance. Hence, reduced transient variations in the supply allow for a lower nominal voltage, potentially leading to reduced total chip power.

For optimum conversion efficiency, even an integrated switching converter will likely operate at frequencies significantly lower than the bandwidth of the supply variations. Thus, in the next part of the talk I will show that instead of increasing the switching frequency and reducing the conversion efficiency of the switching regulator, the low AC impedance delivered by the previously described parallel linear regulator can be leveraged to significantly improve the overall efficiency of the system.

Speaker Biography:

Elad Alon received the B.S., M.S., and Ph.D. degrees in Electrical Engineering from Stanford University in 2001, 2002, and 2006, respectively. In Jan. 2007, he joined the University of California at Berkeley as an Assistant Professor of Electrical Engineering and Computer Sciences, where he is now a co-director of the Berkeley Wireless Research Center. During his time as a student, he held visiting positions at Intel, AMD, Rambus, Hewlett Packard, and IBM Research, where he worked on integrated circuits for a variety of applications, using bulk and SOI processes from 130nm down to 45nm.

Abstract 5.4 – Oral Presentation

Optimization and implementation of a multi-level buck converter for standard CMOS on-chip integration

Eduard Alarcon
UPC Barcelona, Spain

Abstract:. The presentation addresses the fully monolithic integration of a 3-level 2-phase buck converter for DC-DC stepdown conversion in standard CMOS. First it is shown a design-oriented analysis of the converter considering DCM mode (due to PFM operation for low output currents) and with low values of the floating capacitor (to improve integrability). At transistor-level, a self-driving scheme is proposed which allows supplying the tapered buffer drivers from the floating capacitor, thereby reducing the voltage across the power MOSFETs gate dielectric and improving efficiency. The presented converter exhibits enhanced degrees of freedom in the design space defined by the switching frequency, inductor and capacitors values, which have an impact on the achievable efficiency, occupied silicon area and output ripple. An optimized design exploration is carried out for V_{bat} = 3.6 V, V_o = 1 V, I_o = 100 mA, ΔV_o = 50 mV, which yields a converter with the following main characteristics: L= 20.9 nH, C_o = 18.6 nF, C_x = 3.8 nF and f_s = 51.79 MHz (for I_o = 100 mA), a power efficiency of 68.51 % and a occupied area of 3.77 mm2, which results in a clear improvement when the same structured design method is applied to classical Buck converter. Details of the layout design are discussed. Full-transistor level simulation results validate the improved performance and the efficiency model. Experimental results from an implemented IC validate the time-domain functionality of the on-chip converter.

Speaker Biography:

Eduard Alarcón (S'96, M'01) received the M. S. (national award) and Ph.D. degree in electrical engineering from the Technical University of Catalunya (UPC), Barcelona, Spain, in 1995 and 2000, respectively.

Since 1995 he has been with the Department of Electronic Engineering at the Technical University of Catalunya, where he became Associate Professor in 2000. Since 2006 he is the vicedean of international affairs at the School of Electrical Engineering, UPC. From August 03 to January 04, he was a Visiting Professor at the CoPEC center, University of Colorado at Boulder. He has co-authored more than 100 international scientific publications and has been involved in different national and US R&D projects. His current research interests include the areas of analog and mixed-signal integrated circuits and on-chip power management circuits.

He was recipient of the Myril B. Reed Best Paper Award at the 1998 IEEE Midwest Symposium on Circuits and Systems. He was the invited co-editor of a special issue of the Analog Integrated Circuits and Signal Processing journal devoted to current-mode circuit techniques. He co-organized two special sessions related to on-chip power conversion at IEEE ISCAS03 (Bangkok, Thailand) and IEEE ISCAS06 (Kobe, Japan). He was the 2007 Chair of the IEEE Circuits and Systems Society Technical Committee of Power Systems and Power Electronics Circuits. He was the technical program co-chair of the 2007 European Conference on Circuit Theory and Design –ECCTD07 (Seville, Spain), track chair of the IEEE ISCAS 2007 (New Orleans, US) and IEEE ISCAS 2008 (Seattle, US) and IEEE MWSCAS07 (Canada). He served as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS (2006–2007) and for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS (2006–2007). He is currently an Associate Editor of the IEEE TRANSACTIONS CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS

Abstract 5.5 – Oral Presentation

What About Switched Capacitor Converters?

Seth R. Sanders, Elad Alon, Michael Seeman, Vincent Ng, Hanh-Phuc Le
EECS Department, UC Berkeley, USA

Abstract: A detailed analysis enabling a strategic comparison among switched-capacitor converter topologies and also enabling comparison of switched-capacitor topologies with conventional magnetic topologies is outlined. The analysis framework allows a quantitative comparison of the various popular power conversion circuits in terms of their utilization of switch technology and also their utilization of energy storage devices (eg. capacitors, inductors). Roughly, the analysis views a power converter as an ideal transformer with a given or adjustable conversion ratio, with losses modeled with a series output resistance for load-dependent losses, and with a parallel resistive impedance to capture frequency-dependent and static leakage losses. As such, the series output resistance completely captures the main switching losses in a switched capacitor converter that occur in charge transfers among the main circuit capacitors. Significantly, the analysis shows that for a wide range of conversion ratios, ladder and Dickson type switched capacitor converters outperform the conventional buck, boost, and transformer-based converters with respect to their switch utilization. A similar conclusion on reactive component utilization can be made in favor of the switched capacitor converters.

Since switched capacitor converters contain no magnetic devices, they are well suited to integration in a range of CMOS processes. However, many designers have not viewed switched capacitor converters favorably due to potential difficulties in achieving efficient voltage regulation, enabling high current applications, and in fabrication in low voltage processes. Solutions to these potential problems are discussed. Reports on on-going CMOS integration projects targeting three application areas are given. These application areas are in the point-of-load dc-dc conversion function where discrete ceramic capacitors are co-packaged to complete a CMOS-based converter design, in the on-die power train of an ultra-low-power wireless sensor node application, and in the on-die microprocessor voltage-regulation function.

Speaker Biography: Seth R. Sanders received the S.B. degrees in electrical engineering and physics and the S.M. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 1981, 1985, and 1989, respectively. He was a Design Engineer at the Honeywell Test Instruments Division, Denver, CO, during 1981-83. Since 1989, he has been on the faculty of the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, where he is presently Professor. His research interests are in high frequency power conversion circuits and components, in design and control of electric machine systems, and in nonlinear circuit and system theory as related to the power electronics field. He is presently actively supervising research projects in the areas of renewable energy, integrated power conversion, and digital pulse-width modulation strategies and associated IC designs for power conversion applications. During the 1992 to 1993 academic year, he was on industrial leave with National Semiconductor, Santa Clara, CA.

Dr. Sanders received the NSF Young Investigator Award in 1993 and Best Paper Awards from the IEEE Power Electronics Society and the IEEE Industry Applications Society. He has served as Chair of the IEEE Technical Committee on Computers in Power Electronics, and as a Member-At-Large of the IEEE PELS Adcom.

Abstract 5.6 – Oral Presentation

Fast dynamics with non linear control: merits and limitations

José A. Cobos

Centro de Electrónica Industrial (CEI)

Universidad Politécnica de Madrid

ETS Ing. Industriales

José Gutiérrez Abascal, 2. 28006 Madrid (SPAIN)

Abstract: Non-linear control techniques may be very appropriate to optimize the dynamic response of on-chip converters running at MHz. Parasitic effects may limit the bandwidth of linear control and different non-linear techniques, either Digital or Analog, are proposed in the state of the art to speed up the dynamic response. A technique based on hysteretic control of the output capacitor current is presented in this talk. This technique provides very fast dynamics. Merits and limitations of this technique are reviewed.

Speaker Biography: José A. Cobos received the Master and Doctoral degrees in Electrical Engineering from the Universidad Politécnica de Madrid, Spain, in 1989 and 1994 respectively. He is a Professor at this university, since 2001. His contributions are focused in the field of power supply systems for telecom, aerospace, automotive and medical applications. His research interests include low output voltage, magnetic components, piezoelectric transformers, transcutaneous energy transfer and dynamic power management.

He has published over 200 technical papers and holds 3 patents. He has been actively involved in 22 R&D projects awarded with public funding in competitive programs, and 42 direct contracts for research and development for different companies worldwide, including Alcatel, Indra, Siemens, Philips Hearing Implants, Crisa, Tecnobit, Sedecal, Premo and Sener in Europe, Agere Systems, Enpirion, Ansoft and General Electric in US and Cochlear in Australia.

He cooperates regularly with IEEE and other professional associations. He was member of the local organizing committee of PESC'92 in Toledo, and EPE'95 in Seville. He is AdCom member of the IEEE Power Electronics Society (PELS), and Chair of the Technical Committee on DC Power Supply Systems. He is serving as Associate Editor of the Transactions on Power Electronics. He also served as Associate Editor of the IEEE-PELS letters and Associate Editor of the special issue of the Transactions on Integrated Power Electronics. He has advisored 11 Doctoral dissertations, and conducted professional seminars and tutorials in US, Italy, Switzerland, Siria, Mexico and Macedonia.

He received several awards, including the UPM Research and Development Award for faculty less than 35 years of age, and the Richard Bass Outstanding Young Power Electronics Award of the IEEE (year 2000). He served as Vice Dean for Research and Doctorate and currently is serving as Vice Dean of Studies of the ETS Ingenieros Industriales (ETSII) of the Universidad Politécnica de Madrid.

He is Executive Director of the "Sociedad de Amigos de la Escuela" (ETSII) and President of the "Asociación de Antiguos Alumnos" of this school. In 2006 he founded the "Centro de Electrónica Industrial", awarded among the top 5 European universities by the EPSMA (2007), and also awarded with the "UPM Technology transfer award" (2006). He is member and "Roadmap chair" of the European Center for Power Electronics.

PWR SoC 08 | Tyndall National Institute

Session 6: Monolithic Integration vs System in Package

Wednesday, September 24th, 2008 – 8.30 – 12.30

Chairs: Francesco Carobolante, Paul McCloskey, Braham Ferreira

This session will discuss power supply integration in the context of the trade-offs between an "all-silicon" solution and a "discrete in a package" solution. The benefits and the limitations of the two solutions will be explored. Figures of merit will be considered to allow an objective characterisation of the two integration routes for specific applications. The session will also address issues of performance, efficiency, thermal management, EMC, reliability, cost and flexibility afforded by both implementations.

Time	Speakers	Affiliation	Country	Title of the talk
08:30-08:55	Phil Rutter	NXP Semiconductors	UK	Design Considerations for Integrated Power Trains
08:55-09:20	Matthew Wilkowski	Enpirion	USA	Monolithic Integration Vs "System in a Package"
09:20-09:45	Henk-Jan Bergveld	NXP Semiconductors	Netherlands	Integrated inductive DC/DC down conversion for integrated power management using a two-die approach
09:45-10:10	John S. Glaser	GE Global Research	USA	A 1kW, 330V to 50V DC-DC Power Converter with a 30MHz Switching Frequency
10:10-10:40	Coffee/Tea Break			
10:40-11:05	Arnold Alderman	Anagenesis	USA	Update on PSMA Study of Power Supply in Package Vs Power Supply on Chip - PSiP2PwrSoC
11:05-11:30	J. A. Ferreira	Technical University, Delft	Netherlands	Embedded passives in housing
11:30-11:55	Risto Tuominen	Imbera Electronics	Finland	Embedded Silicon in PCB
11:55-12:20	Ron J. Gutmann	Rensselaer Polytechnic Institute	USA	Smart Power Delivery using Three-Dimensional (3D) IC Technology with Arrays of Monolithic DC-DC Point-of-Load (PoL) Converters
12:20-12:45	Michael A. Briere	International Rectifier Corporation	USA	High-Frequency GaN-Based Power Conversion Stages
12:45-13:00	Close of Workshop			
13:00-14:00	Clarion Hotel, Lunch			

Abstract 6.1 – Oral Presentation

Design Considerations for Integrated Power Trains

Dr Phil Rutter
Advanced Devices Group, Power Management, NXP Semiconductors

Abstract: The major improvements in discrete Power MOSFET technology (Rds(on) & Qgd) over the past decade mean that significant improvements in system efficiency cannot be delivered by improvements in silicon technology alone: all sources of power loss need to be addressed and improved. In low voltage, high current DC-to-DC converters (e.g. a VRM), reductions in Qgd have resulted in parasitic inductance (package and PCB) becoming the dominant factor in switching loss.

Integrated Power Trains, which combine power MOSFETs and MOSFET driver in a single package (e.g.. DrMOS), have evolved over the last decade to address this challenge by significantly reducing parasitic inductance. This presentation examines the performance benefit of this 'system in package' approach over a discrete solution and explores how additional performance advantages can be gained by exploiting the physical closeness of driver and MOSFETs. For example, reverse recovery losses can be eliminated by sensing the voltage across the MOSFET silicon and modifying the internal timing of the driver so that no diode conduction occurs in the lower (or synchronous) MOSFET.

When designing a DrMOS like product there are a large number of design considerations / optimisations that need to be addressed and will be discussed in this presentation:

1. Technology choice (i.e. lateral/monolithic vs. vertical/discrete); this is essentially a trade-off between the high cost of incorporating power MOSFETs in an IC process and the expense of multi-chip module assembly.
2. Die size: The optimisation of Rds(on) at the maximum output current will give the highest efficiency at maximum current but at the expense of low load efficiency and rapidly increasing product cost.
3. Gate drive voltage: Again, this is a balance between high and low load efficiency but also dictated by the available voltages in a system, which may not always be ideal.

Looking towards the future, thoughts on how this type of product may evolve will be discussed.

Speaker Biography:
Phil Rutter received his PhD from the University of Manchester Institute of Science and Technology, UK in 1995. Since then, he has been employed by NXP Semiconductors (formerly Philips Semiconductors) working on Power Semiconductor devices. From 1999 to 2006 he was responsible for the development of products combining discrete power devices with control ICs in a single package – a concept now known as DrMOS. Since 2006, he has been responsible for designing next generation power MOSFET technologies. He holds a number of patents concerning the design of multi-chip modules (that contain power MOSFETs), control & driver schemes for power MOSFETs, and power MOSFET device structures.

Abstract 6.2 – Oral Presentation

Monolithic Integration Vs "System in a Package”

Matthew Wilkowski
Enpirion, USA

Abstract: The different trade-off scenarios between market pull versus technology push this would entail the trade-offs between market applications and technical performance for market pull as well as trade-offs between manufacturability and technical performance for technology push.

From the technology push aspect we would discuss the manufacturing issues that must be addressed once the achievable technical performance is demonstrated and the required technical performance is defined.

Conversely from the market pull side we discuss the technical requirements of applications that are large enough to drive the further development of the manufacturing processes.

Abstract 6.3 – Oral Presentation

Integrated inductive DC/DC down conversion for integrated power management using a two-die approach

H.J. Bergveld, K. Nowak, R. Karadi
NXP Semiconductors, Corporate Innovation &Technology, Research, Department Mixed-Signal Circuits and Systems; High Tech Campus 37, 5656AE, Eindhoven, The Netherlands;
HenkJan.Bergveld@nxp.com

Abstract: In many applications, including mobile, automotive, and consumer applications, the voltage of the energy source, such as a Li-ion or car battery, does not match the load voltage. Therefore, circuits are needed that convert the available source voltage to the required load voltage. Additionally, high efficiency of these voltage conversions is desired, e.g. due to long expected run times for mobile devices, improved fuel economy in cars, etc. The drive for efficient voltage conversion rules out the use of linear regulators in most cases. Switched-mode voltage converters using inductors and/or capacitors should therefore be used instead.

Since the number of efficient voltage conversions that have to be performed in a system generally increases, the PCB space occupied by switched-mode DC/DC converters with external passive components will become unacceptably high. Therefore, a clear need exists for small-form-factor high-efficiency DC/DC converters having the necessary passive components integrated within one package. This will eventually enable the integration of a DC/DC converter with the load and consequently the system integration of power management.

Since the loads in most applications are predominantly realized in nm-CMOS technology, the active part of the DC/DC converter also needs to be realized in this technology. However, realizing the relatively area-consuming passive components in nm-CMOS will generally not be attractive from a cost-perspective point-of-view. Therefore, this paper focuses on realizing integrated inductive DC/DC converters in nm-CMOS, where the passive components are implemented in a proprietary passive-integration process technology. The active nm-CMOS die is flip-chipped on top of the passive die to realize a System-in-Package (SiP) DC/DC converter with minimized parasitics. This is important since high switching frequencies (around 100 MHz) need to be used due to the relatively low component values of integrated passives.

The presentation will highlight a first prototype realized by combining a 0.18-μm CMOS die (power stage and drivers) with a passive-integration die (LC output filter and input decoupling capacitor). The passive-integration process features 80-nF/mm^2 trench-MOS capacitors and an 8-μm thick copper top metallization layer. The result is an integrated DC/DC down converter without any external components. A maximum efficiency of 65% at 80 MHz has been achieved for an input voltage of 1.8 V, an output voltage of 1.1 V and an output current of 100 mA. The presentation will also show some first results achieved with a 100-MHz DC/DC converter realized in 65-nm CMOS, which will be assembled in a similar SiP in the near future.

Biography: Dr. Henk Jan Bergveld received the M.Sc. degree (cum laude) and the Ph.D. degree (cum laude) in electrical engineering from the University of Twente in 1994 and 2001, respectively. He joined Philips Research Laboratories in 1994. His work on battery management systems resulted in the Ph.D. degree and the book Battery Management Systems - Design by modelling (Boston, MA: Kluwer, 2002). He is currently team leader at NXP Semiconductors, performing research on integrated power management.

Abstract 6.4 – Oral Presentation

A 1kW, 330V to 50V Dc-dc Power Converter with a 30MHz Switching Frequency

John S. Glaser, GE Global Research Center, 1 Research Circle, K-1 4C22A, Niskayuna, NY 12309, General Electric Company
Email: glaser@crd.ge.com

Abstract: Designers of power conversion circuits are under relentless pressure to increase power density while maintaining high efficiency. A primary path to higher power density is the use of increased switching frequency. In this paper it is argued that the use of switching frequencies in the VHF band (30MHz-300MHz) are a viable path to the achievement of substantive gains in power density. Evidence for this viewpoint is presented in the form of an unregulated 900W prototype dc-dc converter with a 30MHz switching frequency, an input voltage range of 270VDC to 330VDC, and an output voltage of 50VDC. This converter uses a quad module architecture with series input and parallel output to provide acceptable efficiency with the specified input voltage range. Individual modules employ a class EF2 topology to achieve soft-switching on all transitions and wave-shaping for reduced voltage stress. This converter operates with peak output power of 1kW at 330VDC input, has an efficiency of >78% under nominal conditions, with maximum efficiency near 80%.

Biography:

Dr. John Glaser received his BSEE in 1987 from the University of Illinois, Urbana, and his MSEE and Ph.D. in Electrical Engineering in 1991 and 1996, respectively, from the University of Arizona. From 1987 to 1989, he worked at Motorola, where he designed RF power amplifiers for mobile telecommunications applications. From 1995 through 1997, Dr. Glaser was employed by Hughes Missile Systems Company where he researched high voltage converters for TWT amplifiers. Since 1998, Dr. Glaser has been employed by General Electric Global Research, where he has served both technical and project leadership roles on a diverse array of projects including appliance controls, insulation failure detection, power supply failure analysis, battery charge equalization, electronic ballasts, induction heating systems, magnetics for power electronics, high-performance DC-DC converters, and RF power amplifiers for MR imaging applications. Dr. Glaser has published 14 papers in the area of power electronics and has 14 US patents, with several more pending.

Abstract 6.5 – Oral Presentation

Update on PSMA Study of Power Supply in Package Vs Power Supply on Chip - PSiP2PwrSoC

Arnold Alderman
Anagenesis, USA

Abstract:
This presentation provides deeper insight into the data and trends initially reported Power Supply in Package and Power Supply on Chip products and the enabling technologies required for their success. Secondly the presentation provides more recent market data obtained, which enlightens one as to the success and difficulties they are encountering in the marketplace. Thirdly, the material presented examines the advantages and disadvantages these two devices have as competitive power delivery solutions for the integrated circuit. Lastly, information regarding the objectives and scope of the continuing examination of the Power Supply in Package and Power Supply on Chip in PSMA's Phase II project now in progress.

Biography:
Arnold Alderman is founder and president of Anagenesis, Inc. Anagenesis is a technical marketing company that combines both the engineering and the marketing perspective serving power semiconductor companies and power conversion companies manufacturing power supplies, motor controls, electronic ballast, UPS, EPS, and inverters. He co-authored "Market and Technology Report - Power Supply in a Package Power Supply on a Chip" published in February 2008 by the Power Sources Manufacturers Association (PSMA). This was the first such industry report on these two emerging products. He has 16 years of experience in product- and strategic-marketing for power semiconductor discrete and hybrid products at Fairchild Semiconductor and International Rectifier. Mr. Alderman also had 12 years prior experience in commercial power-conversion equipment design, from 2 watts to 12 MVA, in a broad variety of applications including ac-dc power supplies, battery chargers, ac motor control, dc motor control, induction heating converters, and electronic ballast. Mr. Alderman is member of both the Power Electronics Society and the Industrial Applications Society of IEEE. He is a member of the PSMA Board of Directors and is a past Board Chairman He holds a B.S.E.E. from Northeastern University in Boston, Massachusetts, and an M.B.A. from the University of New Haven, in Connecticut. He is the author of one patent, and co-author of three others.

Abstract 6.6 – Oral Presentation

Embedded passives in housing

J.A. Ferreira, J. Popović-Gerber
Electrical Power Processing Unit, EWI Faculty, Delft University of Technology,
Mekelweg 4, 2628 CD Delft, The Netherlands

Abstract: Increasing the level of integration is a means to increase power density, reduce the number of construction parts and manufacturing processes and simplify the assembly of power electronic converters. The key in achieving higher integration levels is in multifunctionality of parts, not only electrical but also packaging parts. The mainstream way is to add more functionality to silicon, by means of monolithic integration or building passive components on the surface of the chip. The approach proposed here is to increase functionality of the housing of semiconductor components by integrating passive components in the housing. Passives, in particular magnetic components, need volume and the housing of semiconductor components has more volume than the chip. Some envisaged advantages of this approach are:

- Surface area/volume of the housing can be used in addition to the expensive silicon real estate;
- Technologies for passive components not limited to silicon processing compatible technologies;
- Better performance – lower winding resistance by using thicker copper conductors/low loss magnetic materials;
- Size reduction – lower number of turns for the same inductance value due to thicker magnetic materials;
- Cost reduction potential – possibility to use lower cost technologies.

Along with the benefits that embedded passives in housing could bring, there are some challenges in implementing thereof that need to be faced. Some of them will be addressed in this presentation:

- Interconnection technologies – suitable technologies for electrical and thermal interconnections between the passive components and the chip need to be explored.
- Miniaturisation technologies for passives – suitability of different materials and technologies needs to be discussed.
- Thermal management – new thermal management techniques are necessary to accommodate the passives and to improve the power density of the power supply in the package.

This approach could be a step towards a fully integrated system-in-package for portable electronic applications, wireless sensor networks and other low power applications driven by increasing functionality, miniaturization and cost.

Biography:

J.A. Ferreira

Braham Ferreira worked in industry at ESD (Pty) Ltd from 1982-1985. From 1986 until 1997 he was at the Faculty of Engineering, Rand Afrikaans University, where he held the Carl and Emily Fuchs Chair of Power Electronics in later years. Since 1998 he is a professor at the Delft University of Technology in The Netherlands.

J. Popović-Gerber

Jelena Popović-Gerber obtained a Dipl.Ing. degree in Electronics, Telecommunication and Control from The University of Belgrade in 2001. From 2001 till 2005 she was with Delft University of Technology pursuing a PhD degree, which she received in 2005. Since 2005 she has been with the European Centre for Power Electronics (ECPE) on the position of a Technology Transfer Coordinator, working on one of the ECPE flagship programmes. Her research interests are packaging and integration of power electronic converters.

Abstract 6.7 – Oral Presentation

Embedded Silicon in PCB

Risto Tuominen
Imbera Electronics Oy
Ruukintie 2, 02330 Espoo, Finland
Phone: +358 207 400 240, Fax: +358 207 400 258
Email: risto.tuominen@imbera.fi

Abstract:
The production of smaller and more complex electronic products places growing challenges for the electronics manufacturing technologies in terms of overall cost efficiency, reliability, suitability for high-volume manufacturing as well as electrical and thermal performance.

To further improve the packaging density, several methods are being developed to embed components inside the package substrate or a PCB motherboard. These technologies enable the utilization of the whole substrate space for component assembly, and are providing an effective solution to improve product performance. One of the main objective in the development of the component embedding technologies is that they enable further product miniaturization without sacrificing the overall cost competitiveness. Also, a typical feature is that the electrical performance can be significantly improved compared to the performance of standard wire bonding technology. A key consideration when embedding the components inside a substrate is to ensure sufficient heat conductivity to conduct the produced heat away from the system.

Imbera Electronics has developed an Integrated Module Board (IMB) technology, which enables the embedding of discrete passive and/or active components inside an organic PCB substrate or motherboard. Imbera Electronics has a long history in high power application area and has developed several thermal via structures to conduct efficiently the produced heat away from the vicinity of the component. This presentation reviews the fundamental considerations when component embedding technologies are adopted. The Integrated Module Board (IMB) process and structure features are review in general technical level, with the aspect of technology utilization in high volume / low cost application area. Also, the usability and design considerations of the IMB technology are reviewed in different application areas. Moreover, some module structure case examples, including for example embedded structures to enhance module thermal properties, are presented and a summary of IMB technology reliability properties is review.

Speaker Biography:
In 1999 Risto Tuominen graduated as a Master of Science from Helsinki University of Technology. His major was Electronics Production Technology and in his master thesis he developed the first Integrated Module Board technology generation. After the graduation he stayed in the university as a project manager until 2001, after which he moved to work as a Research Manager in Finnish HDI-PCB manufacturer Aspocomp Group Oyj. In Aspocomp Group Oyj he worked in the field of embedded active components and majority of his work was to prepare the launch of Imbera Electronics. In spring 2002 he was nominated as the CEO of Imbera Electronics, where his main responsibilities were to industrialize the developed IMB technology and to expand and grow Imbera Electronics operations to support volume manufacturing operations. In 2006-2007 he successfully secured new funding to enable full scale commercialization of company's technology. From 2008 onwards he continued in Imbera as the CTO with key responsibilities of technology licensing, technology road mapping, R&D, development, adoption and ramp up to high volumes.

Abstract 6.8 – Oral Presentation

Smart Power Delivery using Three-Dimensional (3D) IC Technology with Arrays of Monolithic DC-DC Point-of-Load (PoL) Converters

Ronald J. Gutmann and J. Sun
Department of Electrical, Computer and Systems Engineering
Rensselaer Polytechnic Institute
gutmar@rpi.edu

Abstract: Wafer-level three-dimensional (3D) integration offers the potential of enhanced performance and increased functionality, combined with the low manufacturing cost inherit from monolithic IC processing. This technology is both an extension of the IC back-end-of-the-line (BEOL) to enhance interconnectivity and a significant enhancement to present-day wafer level packaging (WLP). The presentation address the problem of power delivery in high-performance ICs with a wafer-level 3D technology platform that includes a stratum of a cellular array of completely monolithic DC-DC converters to provide power locally to the signal electronics. This monolithically integrated, power distribution architecture enables a point-of-load (PoL) DC-DC converter capable of fine-grain power control (both spatially and temporally) for future microprocessors, application specific ICs (ASICs) and system-on-chip (SoC) implementations.

After a review of 3D platforms that enable implementation of such a power delivery architecture, the advantages and challenges of such an implementation are highlighted. A prototype completely-monolithic, two-phase, PoL buck converter cell fabricated with a 180 nm SiGe BiCMOS foundry process is presented, emphasizing the design approach and electrical performance (both static and dynamic). Technologies and designs offering improved power converter performance, specifically conversion efficiency and output current density (output current per unit chip area), are discussed.

Biography:

Ronald J. Gutmann was educated at Rensselaer Polytechnic Institute (RPI), receiving both BSEE and PhD in Electrophysics degrees, and New York University (NYU), receiving a MSEE. From 1962 to 1970, he was at AT&T Bell Laboratories, Lockheed Electronics Company, RPI and the Rensselaer Research Corporation, developing novel semiconductor control devices and circuits. From 1970 through 2005, Dr. Gutmann was on the faculty at RPI, a Professor in the Electrical, Computer, and Systems Engineering Department with teaching and research activities in the areas of semiconductor devices, microwave techniques, and IC interconnects. He has authored or co-authored over three hundred technical papers in these and related fields, has presented approximately 30 invited talks at major international conferences, and is a Life Fellow of the IEEE *for contributions in microwave semiconductor technology*. He has coauthored three books on IC interconnect technology (chemical-mechanical planarization (CMP) and copper interconnects) and recently co-edited a book on 3-D IC technology platforms.

Dr. Gutmann was Program Director of the Solid State and Microstructures Engineering Program at the National Science Foundation (NSF) from 1981-83 and the Director of the RPI Center for Integrated Electronics from 1989-94. He has served on university advisory boards for both SEMATECH and the SRC, and on the IEEE Awards Board.

Abstract 6.9 – Oral Presentation

High-Frequency GaN-Based Power Conversion Stages

Michael A. Briere
International Rectifier Corporation, USA

Speaker Biography: Dr. Michael A. Briere, former Executive Vice President of Research and Development and Chief Technology Officer, joined International Rectifier in November 2003. Prior to his promotion in September 2007, he served as the Executive Vice President, Research and Development, and prior to that, Vice President of Integrated Circuit Development. Among his duties, Dr. Briere was responsible for IR's GaN development between 2005 and 2007. Before joining IR, Dr. Briere held technical and leadership roles at IBM, Cherry Semiconductor, ON Semiconductor, and Vicor, where he led a start-up IC subsidiary, Picor. In addition to his time in the semiconductor industry, Dr. Briere has performed research in physics as a member of the staff at leading research institutes including Hahn-Meitner-Institute (HMI) in Germany and Lawrence Livermore National Laboratory (LLNL) in the United States. Currently Dr. Briere has formed his own executive scientific consulting company, ACOO Enterprises LLC. Dr. Briere earned his Dr. rer. nat. (Doctorate of Science) in Solid State Physics from the Technical University of Berlin and his MS in Physics and BSEE from Worcester Polytechnic Institute in Massachusetts. He served as Associate Adjunct Professor in Physics at the University of Rhode Island. Dr. Briere is an active member of the IEEE and served on the program committee of the International Symposium for Power Semiconductor Devices and ICs (ISPSD).

Poster Session

(topics covered in sessions 1-6.)

Monday (September 22nd)

10:40-11:15; 14:45-15:15; 16:30-17:00

Tuesday (September 23rd)

10:10-10:40; 14:45-15:15

Chairs: Saibal Roy, Maeve Duffy, Terence O'Donnell, Paul McCloskey, Ningning Wang, Fernando Rhen,Cian O'Mathuna

High Efficiency Synchronous Buck Converter using optimised Split-Gate RSO MOSFET

C.F. Tong, P.A. Mawby, J. A. Covington
School of Engineering,
University of Warwick,
Coventry CV4 7AL, UK

***Abstract*— In this work, we have investigated a Split-Gate RSO (Resurf Stepped Oxide) MOSFET for the application of synchronous buck converter. The device showed a remarkable Figure of Merit (FOM). The efficiency of the device responding in synchronous buck converter circuit confirmed that this device is perfect for this application. Simulations corroborate an impressive improvement of efficiency of the VRM in the 5MHz range. The results show that Split Gate RSO MOSFET can achieve an extremely good FOM of 5.83 mΩnC and the efficiency of the circuit at switching frequency of 5Mhz was as high as 80% which makes Split-Gate RSO MOSFET the ideal switch for this kind of application.**

I. Introduction & Simulation Results

Power MOSFETs are widely used as both control and synchronous switch in buck converter. The figure of merit (FOM) use to select Power MOSFET for the efficiency of a buck converter circuit is $R_{ds,on} \times Q_{gd}$. It is well known for a typical trench MOSFET to have a very low conduction loss ($R_{ds(ON)}$) as shown Figure 1. However, trench MOSFETs usually inherit relatively large switching losses due to the higher gate-to-drain capacitance, also known as the Miller charge (Q_{gd}). Goarin et al. [1] demonstrated that a Split-Gate RSO MOSFET, has a doubling in performance over state of the art power MOSFETs for 35 V applications. Figure 2. shows that Split-Gate RSO MOSFET (blue marker) manage to overcome the benchmark of $Q_{gd} \times R_{ds,on}$, setting the new record FOM.

The breakthrough of the Split Gate RSO MOSFET device in reducing the Q_{gd} allow Trench MOSFET to be used in high frequency switching DC-DC circuit, where switching losses might amount to more than 50% losses [2].

The device was investigated using Synopsys MEDICI which yield a low turn-on resistance of 4.17mΩmm^2 as well as an exceptionally low Miller charge (Q_{gd}) of 1.4nC/mm^2. The efficiency (in Figure 3.) of this device running under synchronous buck converter circuit for 5Mhz switching frequency achieves a strong 80% efficiency, assuming all other component is ideal.

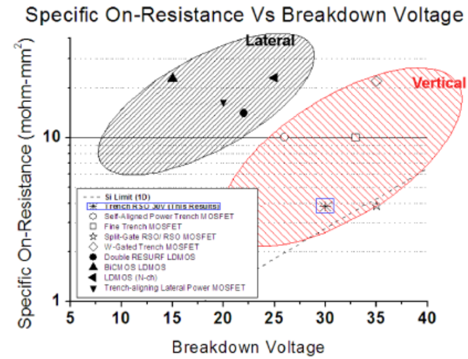


Figure 1. The specific on-resistance is ploted against different type of power switch in 30V range.

II. Conclusion

The Split-Gate RSO MOSFET simulated here is the best structure to date for low voltage DC-DC converter application. In this work, the $R_{ds(ON)}$ achieve 4.17mΩmm^2 with Qgd/A as low as 1.4nCmm^{-2}. With the introduction of this structure as the switch, DC-DC converter will be able to improve its efficiency at high frequency switching due to the lower Q_{gd}. Efficiency is proven to be extremely high achieving 80% for 5Mhz switching.

Acknowledgment

The author gratefully appreciates the financial and technical support from National Semiconductor.

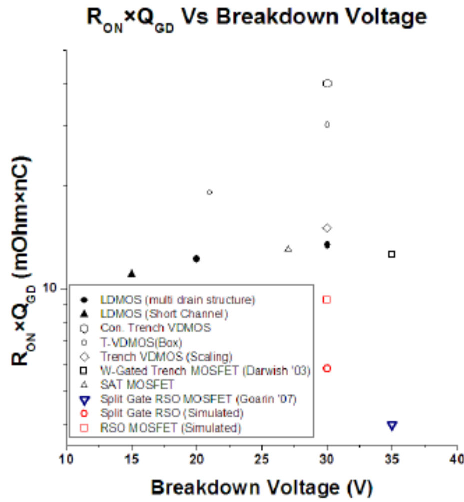


Figure 2. The figure of merit (Ron×Qgd) is ploted against different type of power switch in 30V range.

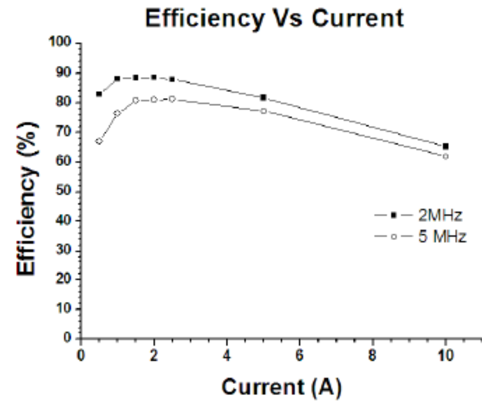


Figure 3. Efficiency ploted against varying load current. (Assuming all other component is ideal).

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An Energy Harvesting System for In-tire TPMS

Thomas Herndl,
Infineon Technologies, Vienna University of Technology, Vestfold University College and SINTEF; Infineon Technologies Austria AG
Babenbergerstraße 10 A-8020 Graz; Tel.: +43 5 1777-11572

Abstract:
State of the art Tire Pressure Monitoring Systems (TPMS) are wireless sensor nodes mounted on the rim. Attaching the node on the inner liner of a tire allows sensing of important additional technical parameters, such as road condition, tire wearout, temperature, tire friction, side slip, wheel speed, and vehicle load. They may be used for improved tracking and engine control, feedback to the power train and car-to-car communication purposes.
Those new features come at a price:
* the maximum weight of the whole sensor system is limited to 5 grams
* robustness is required against extreme levels of acceleration of up to 3000g (g = 9.81 m/s2)
* a 10 years lifetime must be achieved.

Therefore one must get rid of bulky and heavy batteries.
We like to present at the workshop our progress made on the development of a vibration based energy harvester power supply unit for a self-sufficient tire-mounted wireless sensor node, consisting of 2 major building blocks:

Transducer unit:
Vibration energy harvesters can be based on either of three mechanical to electrical conversion mechansims: electromagnetic, piezoelectric and electrostatic. We have designed a MEMS energy harvester for TPMS applications utilizing an electrostatic transduction principle and an electret as a bias for the transducer. Major challenges are the conflict between inertial mass size and the desire for miniaturization, to obtain reasonable efficiency (high unloaded Q and high coupling) and to make a reliable internal biasing through the use of an electret.
Initial simulations of our first degins shows that output power of few uW is possible utilising the motion in a car tire and measurements of a first prototype confirms the workability of our design concept.

Energy conversion unit:
The conversion of harvested energy, provided by a transducer, to voltage levels suitable for energy storage is an other important issue. Challenges are a high conversion efficiency for a wide range of input power levels, integrationability and the support of different types of harvesters. We have developed an integrated supply unit with a power converter for electrostatic or piezoelectric energy harvesters, ultra low power voltage regulators as well as supervisory and management circuits optimized to the requirements of a TPMS based sensor node. Measurement results of the first test chip show proper operation and proves feasibility.

Abstract 3 – Poster Presentation

High Inductance Density Low Profile Inductor Structure for Integrated DC-DC Converter Applications

Qiang Li, Fred C. Lee, David Gilham
Center for Power Electronics Systems (CPES), Virginia Polytechnic Institute and State University, 140 Whittemore Hall, Blacksburg, VA 24061, USA

Abstract: With the increased popularity of portable electronics, improved integrated solutions are desired to improve the low power DC/DC converter technology. In order to reduce converter footprint, 3D integration concept are widely used by people, which design magnetic component as an integratable substrate. In this research area, many different structures are used to design magnetic substrate. From flux path pattern point of view, these different structures can be separated into two types. One is vertical flux structure (e.g. spiral coil and meander coil), whose flux path is perpendicular with the substrate; another is lateral flux structure (e.g. toroidal coil), whose flux path is parallel with the substrate. In order to reduce the inductor size to achieve more compact integrated converter, several low profile structures with different flux path patterns (vertical or lateral) are studied and compared. The study result shows that the lateral flux structure has higher maximal inductance density than vertical flux structure when the core thickness below certain value. Therefore, general speaking it is better to use lateral flux designing low profile inductor due to its higher maximal inductance density. Based on Low Temperature Co-fired Ceramics (LTCC) technology, some lateral flux structures is proposed to increase inductance density for low profile inductor design. A 1.5MHz, 5V to 1.2V, 3D integrated Buck converter with LTCC inductor substrate is designed and fabricated. The full load (Io=15A) efficiency of this 3D integrated Buck converter is around 87%. Comparing with vertical flux, the proposed lateral flux structure can save around 35% footprint. As a result, the integrated converter can achieve 300W/in3 power density.

Abstract 4 – Poster Presentation

Electrodeposited multilayer amorphous alloy suitable for high frequency integrated inductors

Paul McCloskey[a], Brice Jamieson[a], Terence O'Donnell[a], Donald Gardner[b], Mike Morris[c], Saibal Roy[a]

[a] Tyndall National Institute, Cork, Ireland
[b] Intel Corporation, Santa Clara, US
[c] University College, Cork, Ireland

Abstract

The integration of on-chip inductors with magnetic materials into silicon process technology has been a major challenge in the move towards monolithic solutions for wireless microelectronics, power delivery, and EMI noise reduction [1]. Thin film soft-magnetic cores, being central to this integration are now receiving considerable attention [2]. The key material property requirements for these cores to be useful at high frequencies (up to 100 MHz) are low coercivity, high magnetic moment, high permeability, high anisotropy field and high resistivity.
Electrodeposited amorphous CoP has the advantage of high resistivity but exhibits out-of- plane anisotropy and hence very low permeability when deposited on plane surfaces using conventional DC plating unless the thickness is constrained to below 400 nm [3]. In order to have in plane anisotropy and low coercivity for thicker deposits, a multilayer structure consisting of alternating P rich and P poor layers must be created using either pulse reverse plating [4] or pulse plating at two different current densities [5]. Figure 1 shows the Pulse Reveres Plating waveform which consists of a forward on Time ($T_{forward}$) during which Co-P is deposited, a reverse on time ($T_{reverse}$) during which time material is removed and an off time (T_{off}). During $T_{reverse}$ Co is removed preferentially leaving a P rich layer. Figure 1 also shows the dramatic effect of $T_{forward}$ on the B-H loop obtained.

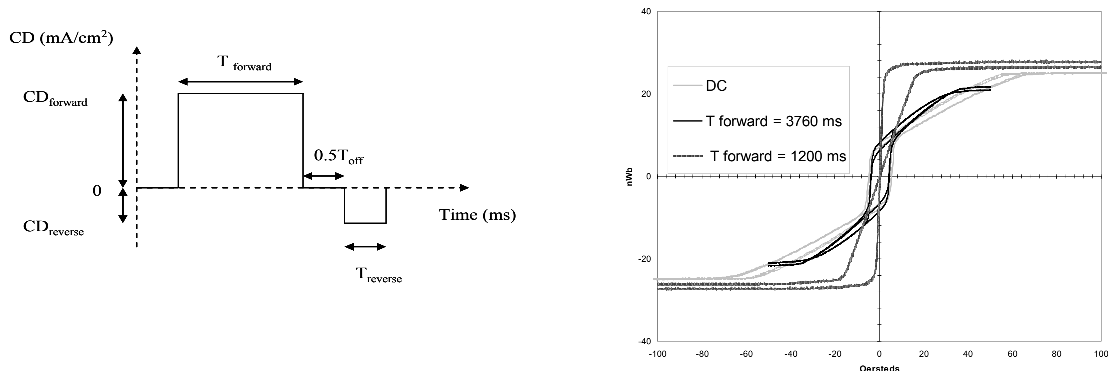

Figure 1: LHS shows Pulse Reverse Plating waveform, RHS shows effect of Forward on Time ($T_{forward}$) on B-H loop.

In order to retain high permeability beyond 100 MHz the material must have both a high saturation magnetisation and a high anisotropy field. In the present work, we investigate using a lower phosphorous bath with the aim of obtaining such properties. Plated multi-nano-layer CoP films have been produced that show good soft magnetic properties, Hc <0.5 Oe, Permeability ~700 holding out to a maximum 103 MHz, Saturation Magnetisation, Bs in the range of 0.9 to 1.2T and resistivity in the range of 116 -136 μOhm cm.

The temperature stability of the magnetic properties is also an important consideration because of the processing steps involved in fabricating an inductor consisting of a magnetic core that encloses the windings. Oda et al [6] used small additions of Tungsten to improve crystallisation temperature of amorphous FeCoP alloys. Tungsten has a large atomic weight of 183.8 and it is thought that its large atomic radii plays a role in bringing about an increase in crystallization temperature. However electroplating baths containing Tungsten have a considerable tendency to be unstable. Rhenium has an atomic weight of 186.2 and Brenner [7] describes how it can be readily co-deposited with Iron group metals. The present work includes the characterisation of a novel electrodeposited alloy CoPRe that shows a considerable improvement in temperature stability in comparison with the normal CoP alloy. Figure 2 shows the coercivity before and after 298°C anneal for various levels of Re. The anneal was carried out under vacuum and consisted of a 125 minute ramp, 30 minute dwell and 20 minute cooling.

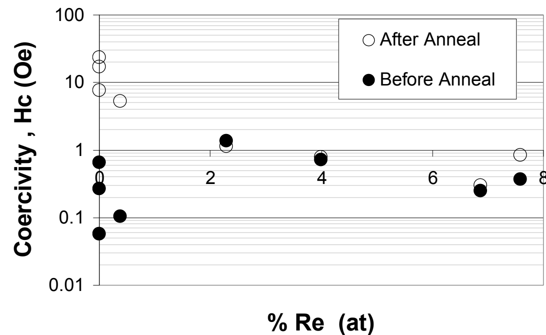

Figure 2:Effect of 298°C anneal

It can be seen that the presence of Re leads to a very significant improvement in the temperature stability of the alloy.

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Abstract 5 – Poster Presentation

3D Integration of Power Supply for Non-isolated Point-of-load Applications

Arthur Ball and Fred C. Lee
Center for Power Electronics Systems (CPES), Virginia Polytechnic Institute and State University, 140 Whittemore Hall, Blacksburg, VA 24061

Abstract: The goal of this project is to investigate, assess, design and implement a methodology for integration of active and passive parts of a buck converter into a small and effective package that addresses electrical and thermal considerations concurrently. The push for integration is brought about by the desire for high power density and small footprint but is constrained by thermal issues. An example design is shown operating at 1.3MHz switching frequency, which represents a good compromise between size and efficiency.

The overall system design methodology is divided into two main parts. One is integration of the active components in which devices are used as bare dies (IR DirectFET®) and are *embedded* in a single layer of aluminum nitride Direct-Bonded Copper (AlN DBC) ceramic substrate. This allows for layering on top and bottom with circuit components, such as an inductor substrate, and yet also integrates thermal management.

The second is the inductor substrate made using Low Temperature Cofired Ceramic (LTCC) process so that we can have a low profile and an advantageous non-linear inductance. The fabricated inductor uses LTCC ferrite tapes built up to the desired thickness, with the silver paste inductor trace embedded in it. Finally, we reflow the active layer with the LTCC inductor and test the integrated converter as a whole.

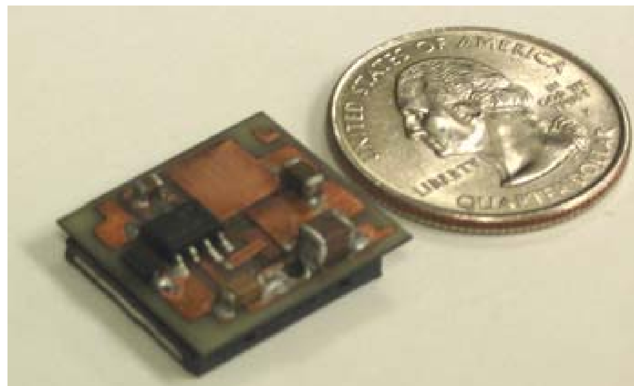

Photo of final product next to an American 25 cent coin.

The advantages and technical highlights of this design are:

1. Small footprint of 3.5 cm^2 and a low profile of 5 mm
2. Integrated thermal management replaces PCB, heat sink, and cooling fan.
3. 260 W/in^3, including all thermal management and necessary capacitors.
4. 20A output with no need for fan or heat sink in 50°C ambient
5. 5V to 1.2V efficiency of 88% at 24A, and 12V to 1.2V of 85% at 24A

Abstract 6 – Poster Presentation

LTCC Technology for Low Profile Magnetics Integration

Michele Lim
VT

Abstract: In power electronics circuits, magnetic components are usually one of the bulkiest components in the circuit. The increasing market demand in low profile electronics provide a strong driving force for low profile magnetics. In low profile power electronics applications where high current or high power capability are desired, for instance in notebook computers and flat panel displays, on-chip integration of magnetics may not be the best option. Hybrid integration of magnetics with active devices provides the other avenue where the requirement for high current and high power can be realized. LTCC technology, being tailored for low profile electronics is naturally an area worth exploring for power electronics applications.

A low-profile power inductor fabricated using low temperature co-fired ceramics (LTCC) technology has been demonstrated to improve the light-load efficiency of a 5 V–to-1 V, 12.5 A buck converter operating with a switching frequency of 4 MHz, without the use of additional control circuitry. Variation in inductor geometry is performed experimentally to study the effects on the light-load efficiency of a converter. By decreasing the conductor width of the inductor, the light-load efficiency can be further improved by more than 30 % over that of commercial inductors having similar full load inductance. An empirical model is developed based on in-circuit large signal measurements to describe the relationship among inductance, average current, and inductor geometry to help in the future design of such planar inductors. In the use of such inductors as substrate, a conductive shield is required to shield the circuitry from the impact of a magnetic substrate. There is a minimum shield thickness required to minimize losses associated with ringing. High shield conductivity is necessary to lower the trace inductance and minimize power loss. Traces should be placed close to the shield to minimize inductance.

Abstract 7 – Poster Presentation

Integrated Power Supply Test Methods Enabled with a Dynamic Current Load Module

Tom Chambers
Teradyne Inc.
Chicago, IL USA

Abstract: System-on-chip or system-in-package switched mode power supplies provide an opportunity for increased test coverage of the DC-DC converter performance. The conventional approach for testing a switched mode power supply is limited by the level of integration of the supply. In the case of a Voltage Regulator Module (VRM), semiconductor manufactures normally test the component blocks separately. Tests like timing and threshold measurements validate the PWM block. RDSon, current Limit, and short circuit limit are typically applied to the gate driver and power FET components. In more integrated implementations, such as cell phone or digital camera SMPSs, a simple functional check is also performed, but validation is limited by the practical difficulty of realizing best performance in a manufacturing test fixture. Examples of these limitations may include off-package power train inductance and relatively high contactor parasitic inductances. Advances in circuit and packaging technologies provide new test opportunities. This poster will present a production test approach of an integrated SMPS enabled by a current level and slew programmable load. The module may be programmed to change current levels between 5us and 100nS in order to emulate a system load of up to 100A. It resides on a characterization or production test board and can be used with automated test equipment instrumentation or bench equipment to enable testing of power supply kick, droop and efficiency. The poster describes the circuit performance and test methods enabled by the module, focusing on the advantages this technique may provide.

Optimization of Magnetic Enhancement Layers for HighFrequency Transmission Line Micro-Inductors

Brice Jamieson[1], Terence O'Donnell[1], Paul McCloskey[1], D.S. Gardner[2], Saibal Roy[1*]

[1] Microsystems Centre, Tyndall National Institute, Lee Maltings, Cork, Ireland
[2]Circuits Research Lab, Intel Labs, Hillsboro, OR, USA

Abstract: The design of integrated micro-inductors has recently begun to look to high-current designs operating at high frequencies (hundreds of MHz). Inductance enhancements of 28 [1] and current capacities of 10 A [2] have previously been reported, however devices showing either high inductance enhancement or high current capacity require very different designs. This work investigates the effect of soft magnetic layer properties and geometry on the optimal inductance enhancement and current handling capability of micro-inductors operating in the hundreds of MHz range.

Transmission line inductors, consisting of a single turn surrounded by a layer of magnetic material, are an interesting structure for low value, high frequency and low resistance inductors. Previous models for such structures have been used to study the inductance enhancement effects of the magnetic layer. In this work these were found to become less accurate when compared to finite-element modeling (FEM) for device heights of above a few µm. To overcome this limitation, an analytic model based on reluctance elements was used which improves on the accuracy of existing models by including both magnetic sidewalls and vias.

High frequency permeability spectra (up to 9 GHz) were measured for a range of soft magnetic materials (NiFe, CoP, and CoTaZr) and these permeability spectra were incorporated into the model. The inclusion of the complex part of permeability allows a detailed analysis of magnetic losses, particularly at the high frequencies desired for future inductor designs. From the measured spectra, the enhancement effects on a transmission line inductor were determined and compared to both FEM and fabricated inductors.

Using the model, a comparison of the candidate materials is presented for transmission line inductor designs. The Q-factor for the inductors is shown to have a maximum value for an optimal magnetic layer thickness which depends on the magnetic properties.

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Abstract 9 – Poster Presentation

INCREASING THE PERFORMANCE OF DPWM AND A/D CONVERTER FOR THE FUTURE INTEGRATED POWER CONVERTERS

J. QUINTERO, P. ZUMEL, M. SANZ, C. FERNANDEZ, A. LAZARO, A. BAUTISTA

GSEP POWER ELECTRONICS SYSTEM GROUP, UNIVERSIDAD CARLOS III DE MADRID

Abstract: Digital control solutions become more attractive than analog controllers for the future integrated power converters because of easy design of more complex control strategies, reconfigurability, and high immunity to noise and low power consumption. However, as the control target and power stage of the converter are inherently analog, digital controllers require the addition of Analog-to-Digital (A/D) converters. This data conversion generates additional problems derived from time discretization and finite word length effects. Particularly, for applications with high switching frequency and tight output voltage regulation, the limited resolution of the Digital Pulse Width Modulator (DPWM) and the sampling frequency of the A/D converter are important issues.

In this paper, a high-resolution DPWM and a high-speed A/D converter are embedded in a low cost FPGA. Only passive external components are added to obtain the A/D converter. Both DPWM and A/D converter are validated in a four phases VRM at 1.2 MHz switching frequency.

The proposed DPWM solution has been implemented by means of a hybrid counter-based DPWM architecture and a specific block available in the FPGA, known as Digital Clock Manager (DCM). Experimental results show a 2.28 ns time resolution, for an application at 1.2 MHz switching frequency, 5 V input voltage and 20 ns clock period. This result improves significantly the time resolution and, as a consequence, the output voltage resolution (15 mV).

As the speed of the A/D is the most important parameter to be taken into account, a flash window A/D converter consisting on several comparators has been considered. The proposed A/D converter scheme combines the internal configuration of the FPGA ports with an external resistor in each I/O port. As a result a very simple and very fast A/D converter is obtained. Moreover, it can be used in “asynchronous like” operation (only one clock cycle of delay), which is very appreciated in non linear control strategies. In this work a linear-non linear compensator has been used to validate both the DPWM and the A/D converter which have been proposed.

Abstract 10 – Poster Presentation

SIMPLIFYING DIGITAL COMPENSATOR FOR INTEGRATION IN PWRSOC AND PSIP

P. ZUMEL, C. FERNANDEZ, M. SANZ, A. LAZARO, A. BARRADO

GSEP POWER ELECTRONICS SYSTEM GROUP, UNIVERSIDAD CARLOS III DE MADRID

Abstract: Digital specific hardware (FPGA or ASIC) for DC-DC power converters is a key technology for the implementation of flexible controllers in PwrSoC and PSiP. Digital controllers provide the ability to change the controller without changing any passive component, while enabling for very interesting capabilities such as interaction with the load, autotuning, adaptation to plant changes, communications, etc. Several of these new features imply the need for changing the transfer function of the compensator, even dynamically. One of the challenges in this field is simplifying the digital circuitry in order to reduce the silicon area and the cost, while keeping configurability and flexibility.

In this work a very simple way to change the transfer function of a digital compensator implemented in specific hardware (FPGA for prototyping and ASIC for final implementation) is presented. The proposed alternative consumes very few digital resources, since it does not need complex digital hardware, such as multipliers, to adjust the frequency location of poles and zeroes.

The main idea is based on the property of discrete transfer function with respect to the sampling frequency: when the sampling frequency is modified keeping the same coefficients of the difference equation, the frequency characteristic of the transfer function is moved in the frequency domain by the same factor. Thus, the compensator is divided in three different blocks: zeroes block and poles block (which can operate at different sampling frequency) and a gain block (adjust by power of two). The transfer function of the compensator can be adjusted by changing these frequencies and the gain. As a result, a compensator with variable transfer function is obtained using very few logic gates.

However, the sampling frequencies cannot be changed arbitrary, in order to avoid some effects of the interconnection of systems with different sampling rate. Therefore, a limited set of compensator designs can be generated from a given compensator by changing the sampling frequency. This limited set is acceptable in many applications.

Experimental results have been obtained from an actual prototype of a buck converter controlled by an FPGA. The experiments show the feasibility of the presented compensator.

Abstract 11 – Poster Presentation

Characterization of Monolithic Coreless Transformers for Power Supply-on-Chip Applications

Rongxiang Wu, Yipeng, Su[a], Johnny K.O. Sin*, and S.Y. (Ron) Hui[a]
Department of Electronic and Computer Engineering
The Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong
Tel: (852) 2358-7052 Fax: (852) 2358-1485 Email: eesin@ust.hk
[a] Department of Electronic Engineering, City University of Hong Kong, Hong Kong

Abstract:
Inductors and transformers are the key components in power supply circuits. The increase in power supply operating frequency to several megahertz reduces the required values of these magnetic components. Therefore, high frequency operation enables the miniaturization and monolithic integration of these magnetic components, and eventually makes the idea of power supply-on-chip (PwrSoC) feasible. Most of the research work on the monolithic integration of transformers for power supply has been focused on thin film micro-transformers. Thin film magnetic core materials are deposited to increase the inductance value, which in turn reduces the device size, and to increase the magnetic coupling. However, the magnetic core materials will also introduce the limitation of magnetic-flux saturation effect and significant hysteresis and eddy current losses. The increase in core loss as frequency goes higher makes the thin film micro-transformers not suitable for future high frequency applications. Coreless transformers on printed-circuitboard (PCB) for power supplies have been shown to be successful. Compared with thin film micro-transformers, monolithic coreless transformers do not only have the advantage of no core loss and therefore no frequency limitation, but also enjoy the advantages of cleanroom compatibility and simpler fabrication process. In this poster, further miniaturization of coreless transformer using silicon substrate for power supply applications will be demonstrated and explored. In the design of monolithic transformers for power supplies, planar interleaved metal-coils is the most popular configuration since it needs only one thick metal layer, although it occupies larger area. In this poster, the modeling and characterization of monolithic coreless interleaved transformers for PwrSoC will be performed for the first time. Different designs of monolithic coreless interleaved transformers are fabricated and characterized, with different sizes, different number of turns, different metal track width and spacing, different inner radius, and different Si substrate resistivities. The metal tracks are fabricated using a 30um-thick electroplated Cu layer which is put on top of a thick oxide layer grown on the surface of the Si substrate.

The authors would like to thank the City University of Hong Kong for financial support of the Strategy Research grant 7002218.

Abstract 12 – Poster Presentation

Micro-fabricated inductors on silicon for DC-DC converters operating at tens MHz

Ningning Wang, Terence O'Donnell, Ronan Meere, Santosh Kulkarni, Fernando Rhen, Jason Hannon, Raymond Foley, Saibal Roy, C. O'Mathuna
Microsystems Centre, Tyndall National Institute, Lee Maltings, Cork, Ireland

Abstract: Trends in the miniaturisation of electronic products, especially in the portable products area has sparked considerable interest in the miniaturisation of the energy processing electronics i.e. the power conversion circuits such as the switched mode power supply (SMPS). In order to miniaturise the power converter, the switching frequency must be increased so that passive components can be miniaturised and integrated. This work focuses on the development of micro-fabriated inductors on silicon for dc-dc converter operating at tens of MHz. Several different variants of the inductors have been designed and optimised for the application in a low power Buck converter operating at 20-30MHz with the inductance varying from 30nH to 200nH. The inductors have been fabricated using a process technique fully compatible with the standard CMOS fabrication. The micro-fabricated inductors have been fully characterized and exhibited good frequency response with the inductance holding up to at least 20MHz. The saturation current of the fabricated devices is up to at least 0.5A. The performance of these on-silicon integrated inductors have been further demonstrated in a DC-DC converter operating at 20 ~ 30MHz. The achieved highest converter efficiency is 74% at 20MHz. The developed technology of micro-fabricated inductor on silicon will enable in future a monolothic solution to power conversion, and realise the concept of a complete "Power-Supply-on-Chip" platform.

Abstract 13 – Poster Presentation

Topology comparison for a system-in-package integrated DC-DC converter for portable electronic applications

F. Haizone*, H.J. Bergveld†, J. Popović-Gerber#, J.A. Ferreira*
*Delft University of Technology, Delft, The Netherlands, †NXP Semiconductors, Eindhoven, The Netherlands, #European Centre for Power, Electronics (ECPE), Nurnberg, Germany

Abstract: Portable electronic devices, such as laptop computers and personal portable electronic devices are battery powered and need power electronics converters as an interface between the battery and the load. To ensure a long battery life, it is important that the power electronic converters operate at high efficiency. The volume available for power electronics is limited which necessitates the use of integration technologies to achieve high power density converters. Integrating passive components in silicon makes monolithic integration of power converters in system-on-chip difficult and hybrid integration in the form of system-in-package where passive components are implemented in alternative technologies and integrated in the package seems to be a more feasible option at present.

In order to integrate passive components in the package they have to be reduced in size, which is achieved by operating the converter at high switching frequencies thus reducing the volume required for energy storage. The switching frequency increase results in the increase of switching losses in the power semiconductors which negatively influences the efficiency. Furthermore, power semiconductor losses are directly dependent on the chip size which in turn influences the cost of the converter. Also, the losses are dependent on the time waveforms of electrical currents and voltages which in turn depend on the chosen circuit topology. This poster will present a topology comparison and the feasibility evaluation for the implementation of a dc-dc converter (V_{in} 3V– 4.2V from Li-ion battery, V_{out} 0.6V– 1.2V, load current<several 100mA). It is assumed that the converter is implemented in 65nm CMOS technology. The topologies will be compared on the basis of conversion efficiency, cost, size, technological feasibility and transient response. Both single-output topologies such as the synchronous buck topology, interleaved buck topology, inductor multiplier topology etc. and dual-output topologies such as the single-inductor-dual output (SIDO) topology will be considered.

Abstract 14 – Poster Presentation

On-Chip Bondwire Magnetics with Ferrite-Epoxy Glob Coating for Power Systems on Chip (SOC)

Jian Lu, Hongwei Jia, Andres Arias, Xun Gong and Z. John Shen

School of Electrical Engineering and Computer Science University of Central Florida, Orlando, FL 32816, USA
Tel: 407-823-0379 Email: johnshen@mail.ucf.edu

Abstract: A novel concept of on-chip bondwire inductors and transformers with ferrite epoxy glob coating is proposed to offer a cost effective approach realizing power systems on chip (SOC). We have investigated the concept both experimentally and with finite element modeling. A Q factor of 30-40 is experimentally demonstrated for the bondwire inductors which represents an improvement by a factor of 3-30 over the state-of-the-art MEMS micromachined inductors. Transformer parameters including self- and mutual inductance, and coupling factors are extracted from both modeled and measured S-parameters. More importantly, the bondwire magnetic components can be easily integrated into SOC manufacturing processes with minimal changes, and open enormous possibilities for realizing cost-effective, high current, high efficiency power SOC's.

A 200-500 mA Monolithic Buck Converter for RF Applications

Jason Hannon, Raymond Foley, James Griffiths, Kevin G. McCarthy and Michael G. Egan
Department of Electrical Engineering, University College Cork, IRELAND, E-mail: jhannon@pei.ucc.ie

Abstract: This work presents a Buck Converter design optimised for a Wideband Code Division Multiple Access (WCDMA) Power Amplifier (PA). The approach taken is to optimise the switch sizing based on the overall power losses for the system including the output inductor. The Buck converter was optimised for 20 MHz switching with an output current of 200-500 mA. For WCDMA, the modulation scheme requires a linear PA which is an 'always-on' architecture. Most of the power demand is for levels below 20 dBm for data and is even lower for voice. Therefore, optimising the converter efficiency for lower loads can result in longer battery life than optimising efficiency for the highest load. The converter's digital pulse width modulator allows for both frequency and duty cycle adjustment, with a maximum frequency of above 30 MHz and a duty cycle range of between 5% and 100% at 20 MHz. The dead time circuit sets dead times from approximately 0 to 5 ns with a resolution of 150 ps. For light loads the high power consumption of high frequency gate drivers reduces efficiency. Therefore to increase efficiency for light and medium loads it is beneficial to use more than one top switch device. An extra top switch was implemented, for light loads the second top switch is disabled which lowers power dissipated from the gate drives and for higher loads the top switch is enabled to decrease on-resistance which decreases power losses. A full chip was designed on a 0:35 ¹m process. Efficiencies have been measured with varied output voltages and also varied switching frequencies. A maximum measured efficiency of 82% was achieved at a switching frequency of 20 MHz.

Abstract 16 – Poster Presentation

CoNiFe and CoNiFe-C films for high frequency application

Fernando M. F. Rhen, Paul McCloskey, Terence O'Donnell and Saibal Roy

Microsystem Center, Tyndall National Institute, Lee Maltings, Cork, Ireland; Email: saibal.roy@tyndall.ie

Abstract: High moment CoNiFe alloy is a potential material for replacing NiFe in the integration onto Si. We have investigated CoNiFe and CoNiFe-C electrodeposited by different plating techniques (PRP and DC) and studied their static and dynamic magnetic properties. CoNiFe(PRP) films with composition $Co_{59.4}Fe_{27.7}Ni_{12.8}$ show coercivity of 95 Am^{-1} (1.2 Oe) and magnetization saturation flux (μ_0M_s) of 1.8 T. Resistivity of CoNiFe (PRP) is about 24 μΩ cm and permeability remains almost constant $\mu_r' \sim 475$ up to 30 MHz with a quality factor (Q) larger than 10. Additionally, the permeability spectra analysis shows that CoNiFe exhibit a classical Eddy current loss at zero bias field and ferromagnetic resonance (FMR) when biased with 0.05 T. Furthermore, dynamic magnetic measurement show a crossover between Eddy current and FMR loss is observed for CoNiFe-PRP when biased with 0.05 T. DC and PRP plated CoNiFe-C, which have resistivity and permeability of 85 μΩcm, 38 μΩcm, $\mu_r' = 165$ and $\mu_r' = 35$ with Q > 10 up to 320 MHz, respectively, showed only ferromagnetic resonance losses. The ferromagnetic resonance peaks in CoNiFe and CoNiFe-C are broad and resembles a Gaussian distribution FMR of frequencies. We found that the incorporation of C to CoNiFe reduces Eddy current loss but also lowers the ferromagnetic resonance frequency.

PWR SoC 08 Tyndall National Institute

Abstract 17 – Poster Presentation

ANALYSIS AND OPTIMIZATION OF HF DC/DC CONVERTERS FOR RF TRANSMITTERS

Malal Bathily[1,2], Frederic Hasbani[1], Bruno Allard[2]
[1]STMicrolectronics (Crolles, France), [2]Laboratoire Ampère (Lyon, France)
malal.bathily@st.com

Abstract:
The trend to full integration of DC/DC converters that switch at very high frequency (few MHz to hundreds of MHz) is limited by the associate high switching losses. This drawback impacts the efficiency of the DC/DC converters and make them irrelevant compared to the LDOs.

In this work, we analyse the optimization of the DC/DC converter key parameters when the switching frequency increases. The influence of parameters that limits the capabilities of the converter (bandwidth, duty cycle range) is described. In the particular case of reference tracking, the need for an adaptive control of dead-times in order to save power, is demonstrated. The variation of the efficiency with frequency increase is analysed in order to determine the efficiency achievable by HF DC/DC converters.

The resonant gate drivers are introduced; their purpose is to lower the switching losses due to a high switching-frequency operation by recovering the energy used
to drive the power switches.

Integration of passives components and reliability improvement by design

Matthieu Nongaillard
Laboratoire AMPERE UMR CNRS 5005
INSA de Lyon
NXP Semiconductors
matthieu.nongaillard@nxp.com

The integration of power converter has been improved particularly due to progress in integration of active components and currently main effort of research concern the integration of passive components. System-In-Package (SIP) could efficiently stack dices in the same package for keeping most suitable integrated technology for each component (picture 1).

Thermo-mechanical stress can damage dice as show on picture 2, where a passive die has been cracked after thermal cycling test. In order to get reliable passive components, we can modify design circuit and process manufacturing.

The cost of a modification for a lithographic mask is much less expensive than a process manufacturing modification. In order to improve the strength of circuits against thermo-mechanical stress, I was charged to investigate design modification and I will propose some new design rules.

Literature does not really cover the thermo-mechanical reliability for silicon dice. Notion of reliability in power electronic is generally about assembly. Only few patents were taken out about stress relief pattern and thermo mechanical stress. Problems of stress within dice can impact the manufacturing yield and lead to important cost of non quality. That's the main reason why these researches are company restricted information.

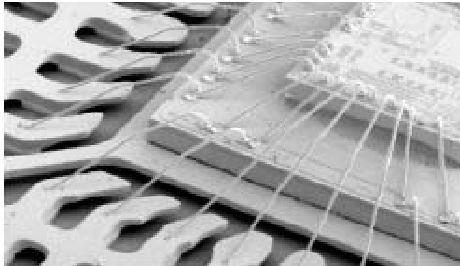
We have already suggested two stress relief patterns:

- Die corners are free of functional structures and the use of stress relief pattern in these areas can complete the seal ring (which is a stack of layer whose protect the circuit). Additional structures can create some conditions of mastered fragility to reduce thermo mechanical stress, and the destruction of these structures doesn't disturb functionalities of the circuit (sacrificial structure).
- In the same way, using slots on the superior metallic layer (picture 4) could improve strength against thermo mechanical stress without cracks.

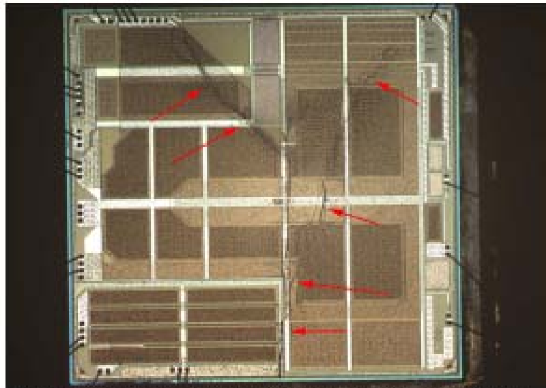
The study has begun by an experimental approach which can cover only several cases because of the manufacturing cost for a demonstrator. FEM (Finite Element Modeling) simulations have been developed to improve the number of evaluation. The results of these simulations will be validated by the experimental approach (model and hypothesis).

The efficiency of a solution for reducing stress is evaluated by the number of defected die and the type of the defect. Experimental results have been obtains by passive thermal cycling between 150°C and -65°C and each die are electrically tested every 100 cycles,

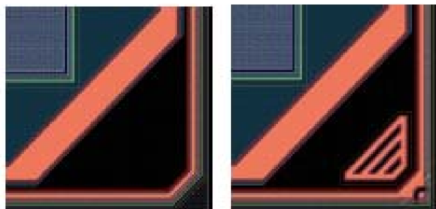
This presentation summary the study, the main approach and the first experimental results and simulations obtained so far.



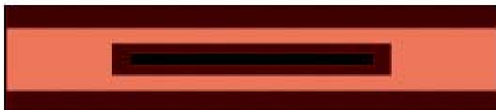
Picture 1: Example of dice stacking used in System in Package



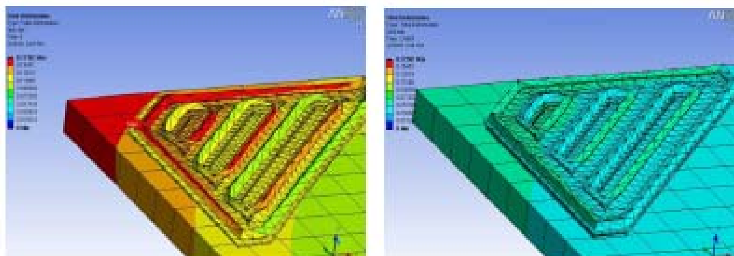
Picture 2: Cracked die by thermo mechanical stress



Picture 3: Corner stress relief suggested (*seal ring*)



Picture 4: Other stress relief pattern (Slot)



Picture 5 : Simulation of TMCL stress in a stress relief pattern

Abstract 19 – Poster Presentation

Spiral type micro inductor with CoNiFe core

J.P Laur, D. Bourrier, M. Dilhan, M. Brunet, T.El Mastouli, J.L Sanchez
Université Toulouse, LAAS CNRS, 7 av. du Colonel Roche, F 31077 Toulouse, France.

Abstract: The necessity to reduce size and weight of electronic devices for embedded equipments increases. Manufacturing of integrated magnetic components on silicon chip dedicated to power conversion becomes then essential. This miniaturization requires developing of new microfabrication techniques and materials that improve the characteristics of micro inductors associated in integrated DC DC converters.

This paper discusses the technologies required to produce a spiral type micro inductor integrated on silicon. In order to be compatible with standard CMOS technology, we investigated a low temperature process using thick photoresists and electro deposition of metallic and magnetic materials.

The structure realized is composed of a copper spiral sandwiched between two laminated magnetic layers. In order to carry out this stack of three metal layers thicker than 60µm, we had to overcome major difficulties. The first one was the realization of the photoresist molds for the electroplating. We have optimized the process of a negative thick photoresist strippable in order to obtain an aspect ratio up to 4. This development allows the realization of a vertical laminated magnetic core with 15 µm wide and 60 µm thick layers spaced by 15 µm. The second difficulty was to optimize the flatness of the stack to keep the photolithography resolution. We have obtained good results by including CMP steps in the process.

Finally, to optimize an electroplating process for the magnetic core, several parameters were investigated by changing temperature, pH, current density of plating process. The electro deposition of thick $Co_{60\%}Ni_{15\%}Fe_{25\%}$ .with optimal magnetic properties (B_{sat}# 2,4 T, H_c 24 Oe) was achieved. In order to integrate on silicon, the influence of organic additives was studied to improve the morphology, to decrease the stress of the plating. The fabricated micro inductors were implemented in DC DC converters. Measurements were carried out at 2MHz and 3MHz. The electrical characterization of the fabricated prototypes exhibits a 1µH inductance value and 1.2Ω dc series resistance value.

Abstract 20 – Poster Presentation

Nanocomposite mesoporous based materials for application in future inductor cores

Jeffrey F. Godsell[a], Keith P. Donegan[b], Joseph M. Tobin[b], Fernando M. F. Rhen[a], David J. Otway,[b] Michael A.Morris[b,c], Terence O'Donnell[a], Justin D. Holmes[b,c], Saibal Roy[a]

a) Microsystems Centre, Tyndall National Institute, Cork, Ireland.
b) Chemistry Department, University College Cork, Cork, Ireland.
c) CRANN, Trinity College Dublin, Dublin, Ireland.

e-mail: saibal.roy@tyndall.ie

Abstract: Recent advances in the field of nano-composite materials have led to the creation of a new class of material with their physical properties controlled on the nanometer length scale. These nanocomposite materials may be produced by a conventional sol-gel synthesis technique without the need for a high temperature processing step; this makes these materials potentially IC compatible. Conventional inductor core material deposition techniques face genuine limitations to their implementation in future high volume manufacturing. An example of such a limitation would be the prohibitive time scales involved in the sputtering of suitable quantities of magnetic material for integrated inductor cores. Sol-gel derived nano-composites can be deposited quickly and in the required thicknesses for integrated inductor core structures. The possibility thus exists to utilise these nanocomposite materials deposited in the form of thin films as integrated inductor core structures. In this work ferromagnetic nanoparticle impregnated mesoporous materials are being investigated for their suitability as a potentially new soft inductor core material. It is envisaged that these materials will exhibit superior soft magnetic properties through the averaging of the grain's randomly oriented magneto-crystalline anisotropy via coupling through exchange interaction. This fundamental level research seeks to produce soft magnetic material properties similar to those of nanocrystalline materials (such as $Fe_{73.5}Si_{13.5}B_9Cu_1Nb_3$) with the notable improvement of IC integration compatibility.

As a first step in this developmental process Ni doped mesoporous silica spheres have been produced. Coercivity and saturation magnetisation for nanometal/mesoporous silica spheres have been measured between 300K – 10K. The doped silica spheres have been analysed based on the principle of superparamagnetism and shown to be in excellent agreement with the theory. Coercivity versus temperature was plotted for a selection of Ni doped silica spheres and the results were fitted to a theoretical equation describing the relationship between coercivity and temperature of non-interacting, monodomain, uniaxial particles. Work is being carried out to produce thin film of nanometal-ceramic composites having superior high-frequency soft magnetic properties in a CMOS compatible technique

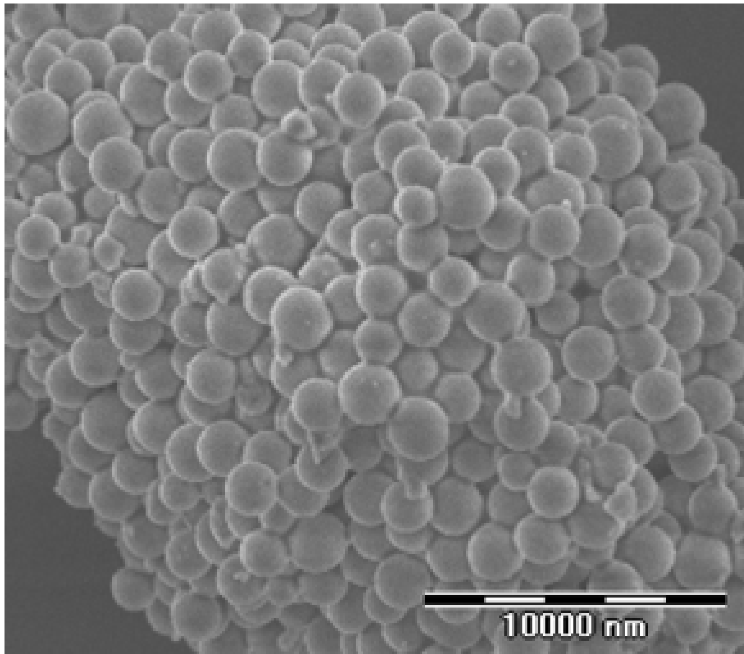


Figure 1: SEM image of silica spheres

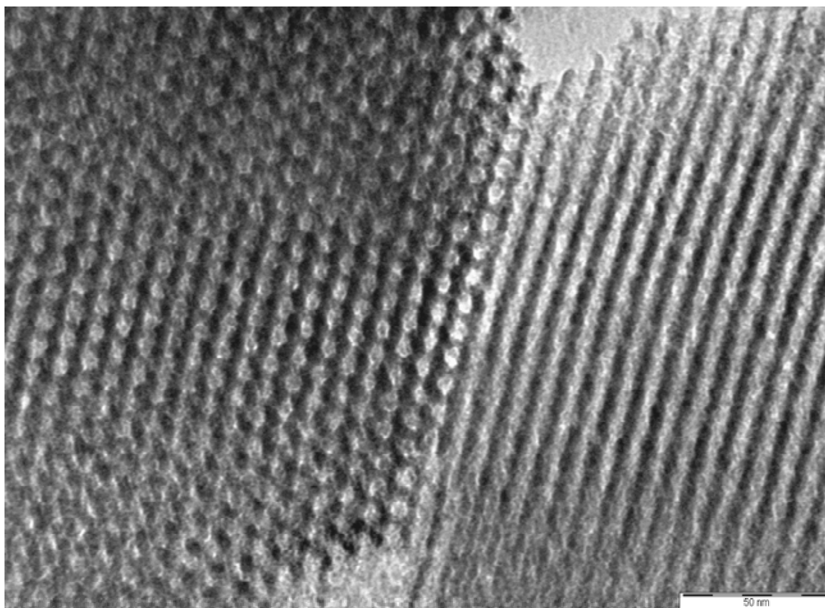


Figure 2: Transmission electron micrograph displaying both head on hexagonal and side view of mesoporous silica.

Abstract 21 – Poster Presentation

Intelligent Power Management Group, University of Limerick: Activities 2008

Dr. Tony Scanlan, Dr. Mark Halton, University of Limerick

Abstract:
The Intelligent Power Management Group (IPMAC) at the University of Limerick, Ireland is involved in the design of key technologies for digital integrated power supply controllers. This poster details active projects within the group for the current year 2008, and outlines a roadmap for future technology development. Current funded projects include the development of improved efficiency power converters for nonisolated POL voltage regulators, particularly at light load. This will be achieved through circuit and advanced control techniques. Coupled with this research strand is the development of event-driven digital control laws for improved VRM transient performance. Complementary to the above activities is the development of integrated circuit and power supply technologies for demonstration and commercialization purposes.

Abstract 22 – Poster Presentation

High Frequency Switching DC-DC Power Converters For Microscale Robots

Christopher D. Meyer, Adura Sopeju, Chris Dougherty, Pengfei Li, Xue Lin, Rizwan Bashirullah, and David P. Arnold

Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL 32611, USA

Abstract: Recent research efforts have aimed at producing microscale robots that can hop, crawl, and fly to perform various tasks. Some approaches have attempted to engineer mechanical microrobots that mimic small birds and insects [1], while others have demonstrated the ability to control the motion of actual insects [2]. Although these efforts have borne novel ideas in microscale ambulation, navigation, sensing, and systems integration, no power supplies yet exist that can provide extended mobility to these tiny microsystems. Small physical size and limited energy resources place stringent requirements on the power supply for low mass, low volume, and high efficiency. Additionally, since these microrobots will likely need to harvest environmentally available energy for extended operations, the power management system must handle a variety of input voltages while supplying power to both low-voltage (control circuitry) and high-voltage (actuator) loads.

The goal of this project is to explore the microrobot power supply problem by leveraging three emerging technologies: ultra-high speed CMOS switching electronics, MEMS-fabricated passive components, and adaptive power processing. Preliminary work has focused on developing a dc-dc boost converter to convert a battery-level (3 V) input to a high-voltage (20-100 V) output for microactuators. Various topologies and CMOS technologies are investigated for handling the high voltage and high switching frequencies (500 MHz) to allow for extreme miniaturization of the passive components. The passives are designed around advanced MEMS fabrication technologies to improve density and efficiency. Parallel-plate, comb, and fractal capacitor structures with high-κ dielectrics are compared in terms of capacitance density and fabrication. Inductor designs aim to maximize Q by electroplating thick Cu coil traces and forming high-frequency cores with polymer-suspended ferrite powders. A hybrid die-level flip-chip integration approach is proposed to merge the custom-fabricated MEMS passives with the CMOS electronics.

[1] R. J. Wood, "The First Takeoff of a Biologically Inspired At-Scale Robotic Insect," *IEEE Transactions on Robotics,* vol. 24, no. 2, pp. 341-347, Apr. 2008.

[2] H. Sato, *et al.*, "A Cyborg Beetle: Insect Flight Control Through an Implantable, Tetherless Microsystem," *MEMS 2008*, pp.164-167, Jan. 2008.

Abstract 23 – Poster Presentation

Integrated Power MEMS Inductor Based on Silicon-Molding Technique

Mingliang Wang[1], Khai D. T. Ngo[2] and Huikai Xie[1]
1 Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL 32611, USA
2 Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, VA 24061, USA
E-mail: bright80@ufl.edu

Abstract: Monolithic integration of DC-DC converters with on-chip inductors has emerged as a viable means to reduce size and increase transient performance for portable electronics applications. High-power-density inductors have been recognized as a barrier for such integration. MEMS inductors have been used for miniaturization and integration, but they have only limited applications in DC-DC converters due to their low power handling capability, high DC resistance, or small inductance. Generally, power MEMS inductors are composed of three metal layers with the top and bottom layer connected by vias. Thick metal layers are needed to achieve low DC resistance and high saturation current. The commonly used method to obtain thick windings is to electroplate metals in polymer molds on top of CMOS substrate, but the thickness of polymer molds is limited by photolithography, especially when multiple metal layers are needed.

In this abstract, a CMOS-compatible process that is capable of fabricating on-chip inductors with low DC resistance and high power density is developed. A unique silicon-molding technique is used to obtain thick electroplated metal layers, in which through-wafer silicon trenches are created by using deep reactive ion etch (DRIE) technology. These deep silicon trenches are used either directly or transferred to SU-8 as electroplating molds. The middle metal layer and the connecting vias are electroplated in the through-wafer molds. The other two metal layers are fabricated on both sides of the wafer. A pot-core inductor with a low-frequency inductance of 134 nH and a dc resistance of 9.1 mΩ has been demonstrated. This process also creates thermal paths for heat dissipation by electroplating metal plugs inside the substrate. The preliminary results show promising applications of this silicon-molding technique in monolithic integration of DC-DC converters.

Synchronization Schemes for High Frequency Hysteretic Controlled DC-DC Buck converters

Deepak Bhatia, Pengfei Li, Lin Xue, and Rizwan Bashirullah
Department of Electrical and Computer Engineering,
University of Florida, Gainesville, FL 32611
E-mail: rizwan@tec.ufl.edu

Hysteretic controlled multiphase switch-mode converters operated at ultra-high frequencies upwards of 100MHz and with peak load efficiencies greater than 80% have been shown to provide extremely fast load response times of 1-5ns. This enables several orders of magnitude reduction in capacitor (and inductor) size, potentially leading to highly integrated near-load power delivery solutions for high performance microprocessors requiring fast entry and exit strategies from multiple supply domains. Unlike the widely used pulse width modulation (PWM) controller, hysteretic control techniques based on a simple feedback loop achieves a near immediate load response without stability issues. However, lack of proper synchronization causes the free-running switching frequency to change with conversion voltage. If kept unchecked, the free-running oscillations may fall in undesired power supply resonance bands created by parasitic package inductance interconnects and on-die decoupling capacitances. This can potentially generate large voltage excursions in the supply network due to high impedance peaks formed by the multi-resonant networks, compromising overall system operation and device reliability. In this work, we present a digital phase lock loop (DPPL) synchronization scheme for hysteretic switch-mode buck dc-dc converters that achieves automatic phase synchronization and constant operating frequency over a wide output conversion range. Owing to the digital nature of the PLL, all parameters including frequency are digitally programmable and locked to an external (or internal) frequency source. We demonstrate a 90-240MHz single phase converter with fast hysteretic control and output conversion range of 33%-80%. The converter achieves an efficiency of 80% at 180MHz, a load response of 40ns for a 120mA current step and a peak-to-peak ripple less than 25mV. The circuit was implemented in 130nm digital CMOS process.

Abstract 25 – Poster Presentation

Voltage Scalable Switched Capacitor DC-DC Converters for Ultra-Low-Power On-Chip Applications

Yogesh K. Ramadass, Anantha P. Chandrakasan

Massachusetts Institute of Technology, Cambridge, USA

Abstract:

Minimizing the energy consumption of battery powered systems is a key focus in integrated circuit design. Ultra-Dynamic voltage scaling (U-DVS) is a popular method to achieve energy efficiency in systems that have widely variant performance demands. In this talk I will present two different designs of voltage scalable switched capacitor DC-DC converters which employ on-chip charge-transfer capacitors. The converters are designed to deliver scalable load voltages from 0.3V up to 1.2V at load currents ranging from 5µA to 8mA. Various techniques to minimize conduction, switching and bottom-plate losses will be discussed. Results from two different switched capacitor DC-DC converters implemented in 0.18µm and 65nm CMOS processes will be presented.

Abstract 26 – Poster Presentation

Loss characterization of magnetic materials for integration on silicon

M. Duffy, C. Collins
Power Electronics Research Centre,
Department of Electronic Engineering,
NUI Galway; Email: maeve.duffy@nuigalway.ie

Abstract: Magnetic components are fundamental to the operation of power supplies, and in order to support their integration on silicon, it's necessary for them to be operated at frequencies in the MHz range. For components with magnetic cores, it is important to ensure that core loss contributions do not offset the advantage of increased inductance / coupling provided. This is particularly true for materials operating in the MHz range, where eddy-current and hysteresis losses become more difficult to control. However, it's often difficult to determine the contribution of core loss over other losses when the device is integrated on silicon and often within a circuit.

This work describes methods for measuring the power loss density of electroplated magnetic alloys that are suitable for integration in silicon. The procedure may be applied to determine which materials have the lowest losses for given core excitation conditions before committing to the integration of devices on silicon. Furthermore, results may be applied to determine the relative contribution of core loss in fabricated devices, so that developments required to provide improved efficiency may be more easily identified.

The measurement procedure is based on the transformer method, where the material sample is excited by a known current supplied on the primary side, and an induced voltage is detected on an open-circuited secondary winding. Compensation for the voltage induced by air-core flux linkage is included, as is the delay between voltage and current waveforms caused by the current probe. Results are presented for a range of alloy samples at frequencies of 3 MHz and 5 MHz.

Abstract 27 – Poster Presentation

Fast response HF DC-DC converter architecture for RF amplifiers based on a multilevel topology

M. Rodríguez, J. Sebastián, A. Rodríguez, P. F. Miaja, D. G. Lamar
University of Oviedo, Spain; Email: rodriguezmiguel.uo@uniovi.es

Abstract: Raising the efficiency of RF transmitters is a topic of intense research activity nowadays. New transmitting architectures based on envelope tracking techniques (ET) have been recently proposed as a solution: the voltage supply of the RF linear power amplifier is varied in order to follow a certain waveform, which corresponds with the envelope of the information signal to be transmitted. In order to achieve this with time varying envelopes that can reach frequencies beyond several megahertz, very special DC DC power converters must be used. These converters must achieve very fast time responses (and very high bandwidths), low output voltage ripples and output powers that can range from hundreds of miliwatts to hundreds of watts.

A new topology suitable to implement these converters is exposed in this work. It is based on two cascaded converters: a multiple output converter which generates different DC voltages and a multiple input converter which provides the fast transient response. This poster focuses on the multiple input topology, which has been called MIBuck (Multiple Input Buck Converter). It has some advantages over the topologies proposed to date: it is robust, achieves very fast time responses and low output voltage ripple, has high efficiency and its control scheme is very flexible. It is oriented to high power transmitters, though it can be easily adapted to low power systems. Also, it achieves high switching frequencies. Some parts of the present implementation are particularly suitable for its integration into a package, specially the driving circuitry MOSFET set.

Abstract 28 – Poster Presentation

Low Parasitic Packaging of Power Modules for High Frequency Operation

Paul McCloskey[a], Ray Foley[b], Virginia Morris[a], Nicolas Cordero[a], Alan Mathewson[a], Cian O'Mathuna[a]

[a] Tyndall National Institute, Lee Maltings, Cork, Ireland
[b] Department of Electrical Engineering, University College Cork, Ireland
Email: alan.mathewson@tyndall.ie

Increasing the switching frequency of switch mode power supplies (SMPS) is an attractive approach for converter miniaturisation as it can lead to a dramatic reduction in the size of passive components required. Considering the simple buck converter, the function of the inductor is to limit the current ripple and it can be readily shown that for a given ripple, increasing the frequency reduces the value of inductance required. This also turns out to be true for the value of capacitance required even after taking into account the impact of the parasitic impedances of the capacitor which can become dominant in the MHz range [1]. Obviously in order to realise the advantages of using a high switching frequency it is necessary to have switches that can operate at high frequency with low loss. This has started to happen at lower currents where for example Enperion offer an integrated converter (EN5366Q) which delivers 6A and switches at 5 MHz. Even at high currents up to 35A the integrated power trains (which consist of a driver and two FETS) available from NXP (PIP12-12M), Renesas (R2J20601NP) and On Semi (NIS3001A) are specified to operate at up to 1 MHz.
However it is also necessary to consider the impact of the electrical parasitics arising from the packaging on the performance of the converter. In order to do this an analytical model of the total losses in a converter was developed [2]. This model takes into account various device parameters such as Rds, Qrr, Coss etc and quantifies their impact on MOS Conduction loss , reverse recovery and ringing turn-on loss etc. It also takes into account the parasitic inductance and quantifies its impact on Pon and Poff loss. The value of the parasitic inductance was determined using the finite element package Ansoft Q3D. The accuracy of this approach for quantifying parasitics was verified using measurements on simplified structures. In order to validate the analytical model a converter was built that could use either discrete MOSFETs and driver or a commercial integrated power train. Taking into account the parasitic inductance arising from the pcb tracks required to connect the discrete components together it was found that the loop inductance was 7.7 nH. This contrasted dramatically with the commercial integrated power train which was found to have a parasitic loop inductance of only 1.4 nH. Both the power train approaches were tested while switching at frequencies of up to 2 MHz. The agreement between modelled and test results for the total converter power loss was found to be excellent. With the thus verified analytic model it was now possible to look at the breakdown of the losses at various frequencies. It was found that for the converter built with discrete components the parasitic inductance started to dominate the loss as frequency was increased. This effect was much less significant for the commercial integrated power train.
The commercial integrated power train was found to utilise multiple wirebonds to make top side connections to the FETs and hence it was thought that he loop inductance could be reduced further if the wire bond connections could be eliminated. The researchers are currently developing a wafer level packaging process which embeds the die in build up layers and eliminates wirebond connections by using plated copper interconnect. Modelling

suggests this will further reduce the parasitic loop inductance loop to a value of 0.6 nH which is expected to improve the high frequency efficiency by around 2%. Furthermore the footprint of the module is expected to be approximately 50% smaller than the commercial integrated power train.

References:

[1] Maeve Duffy, Christina Collins, Fernando M.F. Rhen, Paul McCloskey, Saibal Roy, “High Current Inductor Design for MHz Switching”, presented at IEEE 39thPower Electronics Specialists Conference (PESC) June 15-19, 2008.

[2] Thomas Meade, Dara O’Sullivan, Cristian Achimescu, Raymond Foley, Michael Egan, Paul McCloskey, “Parasitic Inductance Effect on Switching Losses for a High Frequency Dc-Dc Converter”, presented at the Applied Power Electronics Conference (APEC), 24 to 28 February 2008 in Austin, Texas.