

Magnetics on Silicon

An Enabling Technology for Power Supply on Chip

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Section 1: Introduction

In spite of their critical role, most power management systems for electronic equipment are, euphemistically, required by customers “to cost nothing, take up no space and last for ever”. To a large extent, silicon integration has proven to be the main route to achieving these targets, with the integration of control functions and smart power onto silicon allowing dramatic reductions in component count and therefore power supply circuit footprint and cost while at the same time delivering enhancements in manufacturability and reliability.

This paper is concerned with the ultimate scaling of power converter technology to achieve a fully integrated monolithic solution that can be referred to as Power Supply-on-Chip (PSOC) as depicted in figure 1. A further evolution of this concept would be the System-on-Chip (SoC) whereby the load and power supply are incorporated within the same monolithic unit.

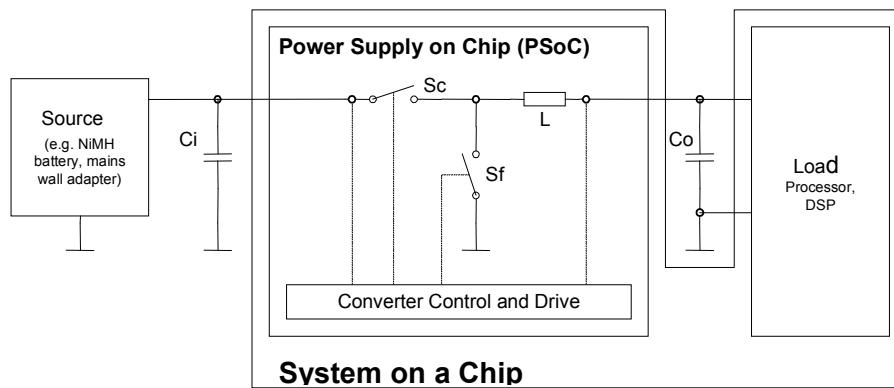


Figure 1: Simplified schematic block diagram of the concepts of Power Supply-on-Chip (PSoC) and Power System on Chip (PSoC)

Section 2 of the paper introduces a number of key technology trends that will drive the performance specifications of power converters over the next decade. These trends clearly lead to the need for multi-megahertz converters and the resulting miniaturisation of the passive components. This section then focuses on the main theme of this paper, the potential for integration of magnetic components onto silicon through the use of thin film permalloy materials instead of the ubiquitous ferrite materials.

Section 3 begins with a comprehensive review of the state-of-the-art in integrated magnetics research worldwide. This is followed by an overview of existing processing technologies and the specific ideas being pursued by the authors to develop low loss, magnetic components on silicon. The section finishes with an outline of the research challenges ahead for magnetics on silicon.

Section 4 focuses on the impact of magnetics on silicon on the other PSOC components. Clearly, magnetics is only one element of the PSOC story. PSOC building blocks can be categorised into power stage blocks and power control blocks. Power stage blocks include the active switches as well as the passive energy handling components for energy storage (i.e. inductors and capacitors) and energy transfer (i.e. transformers). The traditionally analogue building blocks used for power converter control are anticipated, over the coming years, to be replaced by digital solutions that will be more amenable to multi-megahertz switching frequencies. Section 4 introduces a discussion on the current status of

technology in power switches, control and capacitors and in the context of future requirements for multi-megahertz converters. System integration or packaging issues are also discussed in this section.

Section 2: Technology Drivers and Trends in Power Converter Specifications

In 2000, Huljak et al, presented a concise roadmap of the performance and technology developments required in distributed/point-of-load DC-DC converters over the 10 year period, 1998 to 2008. The study emphasised the need to reduce power converter size by increasing converter frequency up to 10MHz by 2008 [1]. Moving to such multi-megahertz converters would enable the reduction in values, and therefore the miniaturisation, of the bulky passive components that are needed for energy storage or filtering and energy transfer.

A review of data from the International Technology Roadmap for Semiconductors for the hand-held electronic product sector confirms the trend, if not the exact figures from Huljak's study [2]. Based on this data, the graph in figure 2 plots the estimated trends in output power, voltage and current for a single buck DC-DC converter supplying power to the digital section of a handheld electronic product. The general trend is an increase in power consumption up to 3Watts, with a decrease in voltages (down to 0.8 Volts in 2010) resulting in an increase in the output current from 2 to 5 Amps.

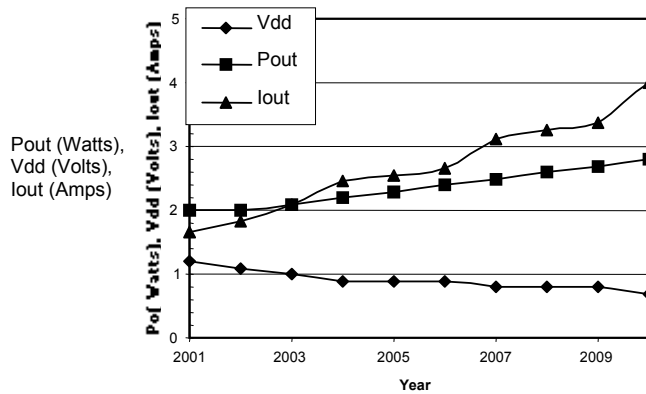


Figure 2: Estimation of the output power, voltage and current for a single buck converter supply in handheld electronic products. All data is based on the ITRS2003 roadmap.

For illustration purposes, given the above estimates for DC-DC converter power, current and voltage, it is relatively easy to determine, for a given switching frequency, the inductance and capacitance values required to satisfy any given specifications for current and voltage ripple. If converter switching frequency remains constant at 1MHz then, given the voltage decrease and current increase in figure 1, the capacitance requirements will increase by a factor of 2.25 by 2010 while the inductance will reduce by a factor of 2.

Clearly, to achieve miniaturisation, a decrease in both the capacitor and inductor values can only be achieved by a significant increase in the converter switching frequency. The graph in figure 3 plots the changes in inductance and capacitance, up to 2010, based on Huljak's assertion of a converter switching frequency of 10 MHz by 2008. In order to achieve comparable reductions in both inductance and capacitance, the current ripple specification is assumed to reduce by 1% each year from a value of 20% in 2001. In this case, by 2008, required inductance values will be 5 % of the 2001 values while capacitance values will have decreased to 20 % of the 2001 values, at a current ripple of 13%. Even assuming a more conservative switching frequency increase to 5MHz in the same period would result in reductions of inductance and capacitance by a factor of 8 and 2.5 respectively. The graph also includes some data points for the switching frequency of low power dc-dc converter products (less than 1 A output) released in recent years. The data points correspond to maximum specified switching frequency as specified on the data sheet. This data would indicate that trends in switching frequency indicated in the graph are actually occurring in practice.

In the context of this paper, multi-megahertz converters raise the issue of availability of suitable magnetic materials – the capabilities of the ubiquitous sintered ferrite needs to be re-assessed in terms of its suitability to deliver high performance, miniaturised magnetic components in the range 5 to 10MHz and higher. The graph in figure 4 compares the power loss in ferrite to that possible with thin film permalloy material over the 10 to 100mT range at two representative frequencies, 2MHz and 10MHz. For thin film materials, which generally have much higher conductivity than ferrites, the eddy current loss is controlled by the film thickness. In general, significant eddy currents are not generated if the film thickness is less than one skin depth [2]. For the graph in figure 4, the thin film is assumed to be a film of permalloy, with a thickness of 0.5 times the skin depth (i.e. 3.5 microns for Ni80Fe20 permalloy at 2 MHz and 1.6 microns at 10MHz

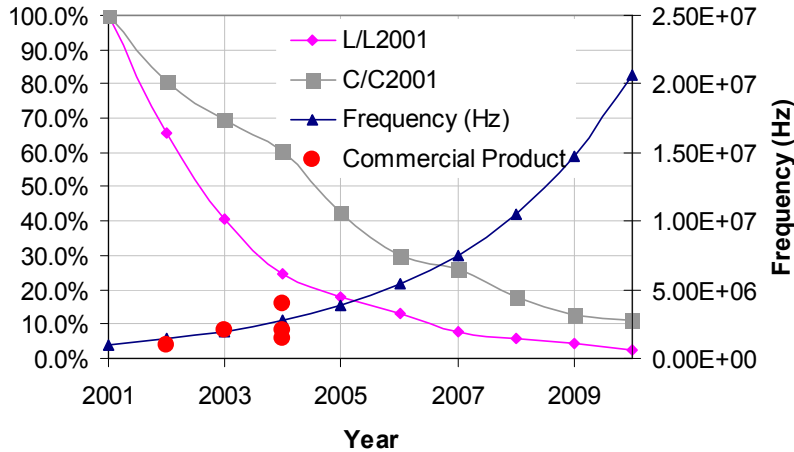


Figure 3: Impact of increase in converter switching frequency on the relative value of passive energy storage elements over the period 2001 to 2010 for a single phase, buck converter in hand-held product with output power, voltage and current as shown in figure 1. The graph is based on data taken from the ITRS2003 Technology Roadmap and assumes an output voltage ripple of 1%, and a current ripple that decreases by 1% each year from a value of 20% in 2001.

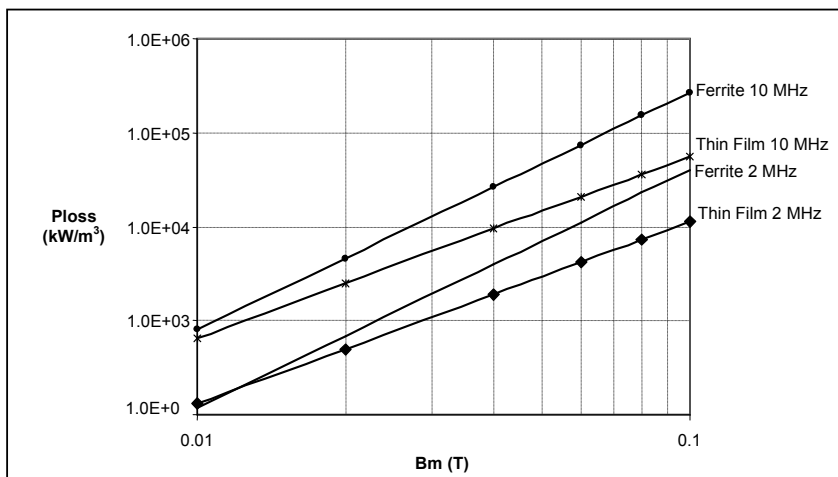


Figure 4: Comparison of core loss vs. frequency for thin film and ferrite. The ferrite core loss is plotted using the Steinmetz equation with published coefficients for the 4F1 ferrite from Ferroxcube. The thin film core loss is plotted using a calculation for eddy current loss [2] and an estimation of hysteresis loss based on the measurement of the BH curve on a toroidal thin film sample.

The graph shows that the core loss density in thin films can be significantly less than that in the ferrite at high flux densities. As an example, at 100 mT, the core loss density in the thin film material is approximately 4-5 times less than that in the ferrite at both 2MHz and 10MHz. It is also worth noting that higher flux density levels can be achieved in the thin films as their saturation flux density is generally in the 1 to 2 T range, compared to 0.3 to 0.4 T for ferrites. Both of these factors imply that greater power densities can be achieved with thin film cores, as the operating flux density can be higher than in ferrite and therefore the cross-sectional area of the core can be smaller.

However, although the power loss density in the thin films can be significantly less, this can only be achieved if the film thickness is of the order of several microns. Therefore the total core thickness (likely to be of the order of several tens of microns) must be achieved by building up multiple laminated thin films. This presents one of the key technological challenges in micromagnetics - how to achieve an adequate overall core thickness, built up from multiple laminated thin layers.

From a manufacturing perspective, thin film magnetic materials offer a further advantage over ferrites as their processing, either by sputtering or electroplating, is compatible with high volume semiconductor manufacturing. This fact, and the reduction in passive component values that result from increased converter switching frequencies, allows the realistic consideration of the functional integration of the passive components with the active silicon devices in the converter. This leads us to the concept of "Power Supply-on-Chip" or "Power System-on-Chip" (PSOC), whereby a silicon-based monolithic integrated converter, integrates many, or all, of the building blocks required to constitute a switching power converter onto a single silicon chip as illustrated in Figure 1.

Section 3: On-Chip Magnetic Components

State-of-the-art Technology Review:

The integration of inductors on to the Silicon substrate using thin film techniques was attempted as early as 1970 [4], although at that time the fabrication was hampered by difficulties in the technology. Much of the technology subsequently used for the fabrication of thin film magnetics, and in particular the developments in magnetic materials, came from the recording head industry, where similar structures are required for the write heads in magnetic recording. In later years many of the techniques used for thin film magnetics, have come from developments in the area of MEMS processing, where for example electroplating techniques for the deposition of thick metal layers have been developed.

Over the last 20 years, the majority of the research work on thin film magnetics, has focused on the integration of inductors into low power, non-isolated converters. Among the most significant contributions to this research has been the work of Sato et. al.[5], Sullivan [6] and Ahn [7],[8]. The closest thing to a fully integrated dc-dc converter including an integrated inductor has been developed by researchers from Fuji Electric [9] who demonstrated 1 Watt converter contained an IC with integrated power switches, control circuitry and an inductor fabricated on top of the IC. Although most of the research has focused on the integration of magnetics for low power converters with currents typically less than 1 Amp, Sullivan et al have investigated the use of integrated inductors for the supply of power to microprocessors, where the overall current requirements may be of the order of hundreds of amps. Single "V-groove" inductors, with an inductance of approximately 6 nH have been designed to carry currents of up to 7 Amps [18].

Work has also been done on the integration of micro-transformers for power applications [10] - [16], although many of the papers only present small signal transformer characteristics (inductances, coupling factors, gain, etc.). Results for efficiency in a power converter have been given by Sullivan et al. [10]; Mino et al. [11] and Brunet et al. [12]. Researchers from NTT, Japan [11] have demonstrated a micro-transformer integrated on to the same silicon substrate as schottky diodes. For a transformer, the performance can be defined by its efficiency, with ideally, an efficiency greater than 95% as the target. The highest value of efficiency reported for a fabricated micro-transformer has been 61%, for an output power of 1.9 Watts operating at 8 MHz [10]. It is clear then that significant improvements are required in the thin film magnetics technology in order to successfully integrate high performance micro-transformers.

The main challenge for the integration of magnetics is to find a cost effective means of integrating the magnetic components onto the silicon substrate, while achieving adequate performance. For a power inductor, adequate performance means achieving the required inductance in as small an area as possible while keeping losses as low as possible. Since a typical power inductor will carry a dc current with an ac ripple, the losses will in general consist of DC winding loss, AC winding loss and core loss. In order to have adequate performance then a power inductor must have a low dc winding resistance, and must limit ac winding and core loss. There are therefore several figures of merit which can be considered for power inductors. These include the inductance achievable, the dc resistance, the ac characteristics and maximum dc current which can be carried before saturation. The ac characteristics of an inductor can be characterized by the Q-factor, defined as the ratio of inductive impedance over resistive impedance.

The graph in figure 5 compares the inductance values achieved using thin film inductors, to those required assuming the voltages, currents and frequencies used in figures 2 and 3. The plot in the figure shows that the actual inductance values achieved are adequate to meet the needs of switching converters in the 1 – 10 MHz range.

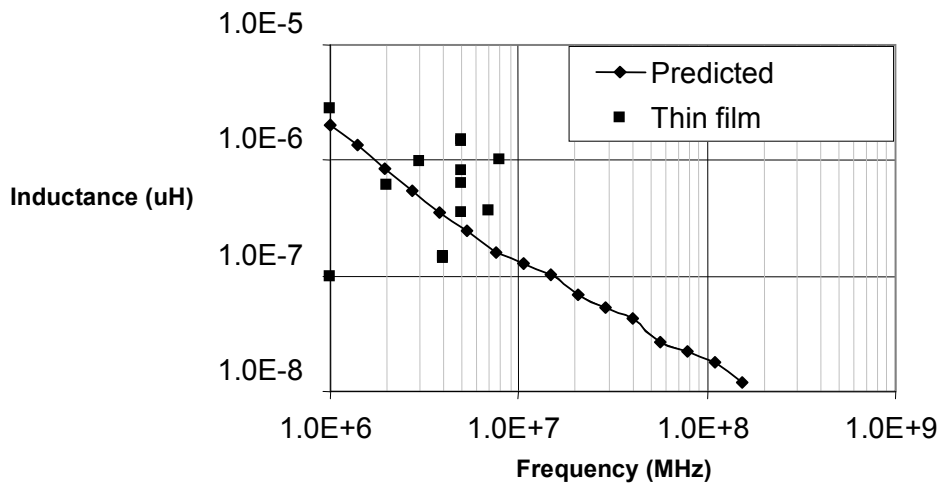


Figure 5: Comparison of the inductance values achieved using thin film inductors, to those required assuming the voltages, currents and frequencies used in figures 2 and 3.

The integrated inductors plotted in the above graph, have achieved inductance per unit area values in the range 20 to 40 nH/mm² for winding resistances less than 1 Ohm. The graph in figure 6 compares the state-of-the-art in micro-fabricated inductors, in terms of inductance and dc winding resistance achieved, to that available from commercial wire wound inductors.

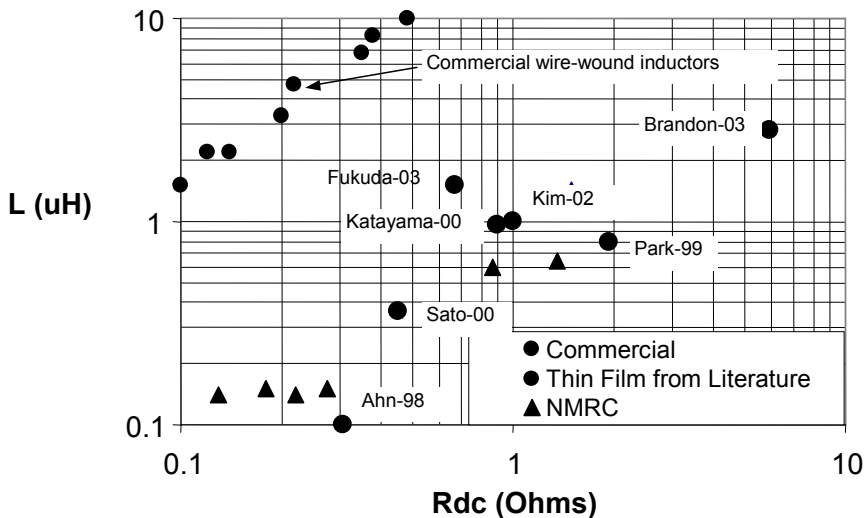


Figure 6: Comparison of the state-of-the-art in micro-fabricated inductors, in terms of inductance and dc winding resistance achieved, to that available from commercial wire wound inductors.

As the graph shows, in all cases the dc resistance of the inductor windings is greater than 100 mΩ with the majority being greater than 500 mΩ. Most of the microinductors reported in the literature have operated at currents of between 0.5 and 1 Amp and, in general, the current is limited to these low values by the winding resistance and also by saturation in the thin film core. However, if we consider an output current of 3 Amps and an output power of 3 Watts, then the dc resistance alone of the inductor is required to be less than 17 mΩ in order that the inductor dc loss account for less than 5 % of the losses. Even this somewhat arbitrary figure of 5 % loss in the inductor dc resistance is probably not acceptable. Clearly then looking at the data in figure 6, it can be concluded that the dc resistance of integrated inductors must be significantly improved if the higher current handling is to be achieved.

In order to compare the ac characteristics of integrated inductors, the graph in figure 8 compares the Q factor of fabricated inductors from the literature, including those fabricated by the authors, to commercially available wire-wound inductors.

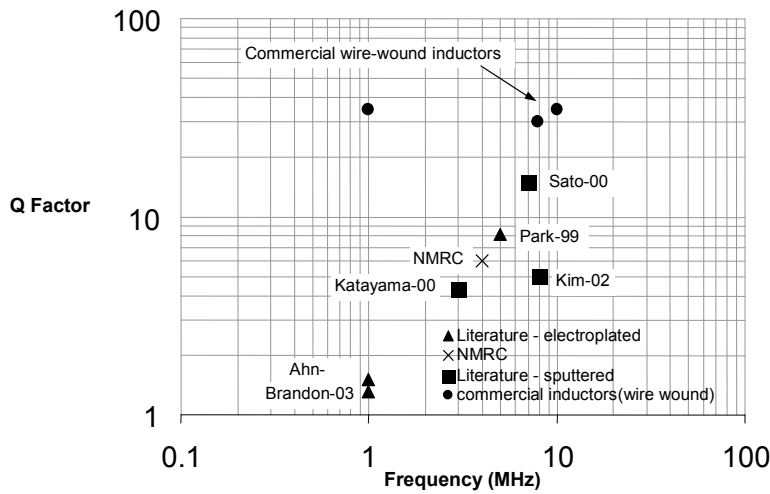


Figure 8: Comparison of Q-factors for integrated inductors and commercial wire-wound inductors.

The graph shows that all the micro-fabricated inductors require improvement in order to attain the Q-factors achievable from wire-wound chip inductors. The discrete, low power, wire-wound inductors can achieve Q-factors of 30 – 40 while the highest Q-factor reported for a micro-fabricated inductor is 15 at 7 MHz [5] and this has been achieved using laminated, sputtered magnetic material, which has a relatively high resistivity ($> 300 \mu\Omega \text{ cm}$). The main limiting factor for the Q-factor is probably the limited core thickness and losses, as inductors using high temperature fired, thick screen printed, ferrite layers with micro-fabricated coils with Q-factors as high as 70 have been reported.

As mentioned previously, most of the integrated inductors fabricated to-date have had current handling capabilities in the 0.5 – 1 A range and lower dc winding resistance is required if higher currents are to be handled. For most of the inductors the current handling is also constrained by core saturation. Core saturation is commonly counteracted by the use of a gap in the core. However the use of a gap decreases the achievable inductance, so that more core cross-sectional area (i.e. thicker or wider core) is then required to achieve adequate inductance. This suggests that in order to increase current handling, both thicker winding and thicker cores are required.

The primary challenge is therefore to develop a material and/or a technology that can be used to deposit thick layers of magnetic material (tens of microns thick), where either the material is highly resistive or, alternatively, a laminated magnetic material can be deposited cost effectively. It would clearly be

more advantageous from a cost perspective point of view to be able to use a single thick layer of magnetic material. Although this paper does not address the cost of the integrated solution, it can be imagined that cost will depend on a number of factors including the number and complexity of the process steps, the die area required, and the volume of the product produced. Also for any particular application there are likely to be cost trade-offs which must be analyzed in terms die area vs. number of process steps, i.e. for any particular application is it more cost-effective to achieve the inductance with a large footprint area and low thickness core (few process steps) or with a small footprint area and a large number of process step.

If the required inductance value decreases, then it may be asked whether a magnetic material is required at all in order to achieve the inductance. If the switching frequency of the converter can be increased sufficiently, then it may be possible to achieve the required inductance without the use of magnetic material [18]. For example, a microinductor of 100nH can be quite easily achieved in a 5 mm² area of silicon. Therefore, it is reasonable to suggest that magnetic material could be dispensed with at frequencies in excess of 10 MHz. However, implementation of the power inductor using standard CMOS metallisation is still unlikely to be feasible, due to the requirement for low resistance coils for carrying high currents. Fabrication of the inductor is therefore likely to still require a post process using thick copper metallisation. In any case, the use of a magnetic material is desirable if it leads to a size reduction in the inductor and if it gives an improvement in EMI characteristics.

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Process Technologies for Micromagnetics:

The performance of integrated magnetics is very much linked to the technology used for their fabrication. The integration of magnetic components onto silicon is generally accomplished by depositing layers of conducting, insulating and magnetic material using semiconductor fabrication techniques such as sputtering, spinning or electroplating and the sequential patterning of these layers using photolithography.

From the point-of-view of miniaturization and integration, we would ideally like to be able to achieve as high an inductance as possible in as small an area as possible. The use of magnetic materials is required in order to achieve this. However, the inductance values achievable are limited by the technology. To maintain compatibility with IC processing, fabrication temperatures must be low (e.g. less than 450°C), which rules out the use of sintering techniques, and thus ferrites, for the magnetic material. Thus, the magnetic materials are deposited using either sputtering or electroplating techniques. The thickness of the layers of magnetic material that can be deposited is therefore limited, by both the deposition technique and the properties of the magnetic materials. For example sputtering techniques are most suitable for the deposition of thin layers (maximum several microns). For electroplating, the materials that can be deposited are, generally, relatively conductive, so that only thin layers (5 to 10 μm) can be used if the eddy current loss in the material is to be controlled. This generally results in the value of inductance that can be feasibly integrated being relatively low.

The second challenge for the functional integration of magnetic components on silicon is achieving sufficiently low winding resistance. This requires the use of thick copper conductors so the only feasible techniques for deposition of the conductors is electroplating. With the majority of integrated magnetic components fabricated to date, it has been difficult to achieve winding resistances of less than 1 Ohm while still maintaining a high inductance. This results from the fact that there is a trade-off between the higher inductance and the higher winding resistance that results from increased number of turns. The challenge here is to achieve the low winding resistance so that current handling can be increased while at the same time achieving high inductance.

Processing for Low Loss Thin Film Magnetics:

The authors research in the area of integrating magnetic components has focused on developing technology that can address these two challenges - deposit thick layers of magnetic material (tens of microns thick) and achieve low winding resistance. The image in Figure 7 shows a cross-section through a micro-inductor fabricated by the authors.

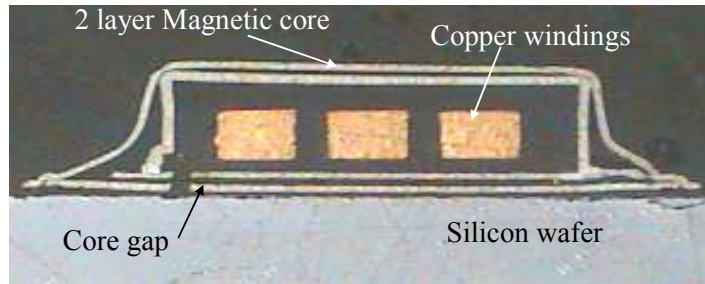


Figure 7: Cross section through a fabricated micro-inductor, showing three turns of copper conductors sandwiched between a two-layer, laminated magnetic core. The core is formed from a 45:55 alloy of NiFe. The inductor footprint area is 5.7 mm^2 .

The device consists of a race-track shaped copper coil sandwiched between the magnetic core [12]. The magnetic core consists of two layers of electroplated NiFe alloy, separated by an insulating layer, essentially forming a two-layer, laminated core. The thickness of each magnetic core layer is approximately 5 microns. The copper conductors are 60 microns thick, with a separation between turns of 35 microns.

This construction has been developed in an attempt to address some of the issues described above. In particular, the laminated magnetic core is used in order to achieve a thick core without introducing significant eddy current loss at higher currents. In the approach adopted here, the entire core, both magnetic material and insulating layers, are deposited by electroplating techniques, so that thick layers can be deposited in a relatively cost-effective manner compared to multi-layer sputtering. The thickness of the copper conductors is 60 microns in order to target low winding resistance. Winding resistances of less than 200 m Ω have been achieved for inductors, as shown in figure 6. High aspect-ratio (ratio of winding thickness to width) conductors have been used in order to increase the conductor cross-sectional area without increasing the footprint area of the device [20]. This also ensures that power density is not reduced due to an increase in the device footprint.

As seen in the plot, the technology developed by the authors has achieved relatively high Q-factor (i.e 6) for gapped micro-fabricated inductors with a current handling capability of approximately 0.7 A. An improvement in the properties of the electroplated magnetic material is required to further increase the Q-factor. It is also worth noting that the same basic technology can be used at significantly higher currents if the application only requires a small value of inductance (e.g. tens of nH). The authors have recently collaborated in the application of the technology described above, to fabricate a 4-phase coupled inductor (with 40 nH per phase), with a designed current handling capability of 10 Amps [25].

Future Challenges:

The magnetics on silicon technologies described above provides a basis for addressing the challenges of fabricating high performance magnetic components on silicon. It can currently address inductance values of up to 1 μH with current handling of less than 1 Amp, making it suitable for low power converters, such as those in hand-held products. However, further improvements are required to achieve a widely applicable technology platform for micromagnetic components.

At higher currents, developments in magnetic materials are needed to achieve the required inductance per unit area. Distributed gap magnetic materials, such as granular or ceramic/magnetic composite magnetic materials [24] may be more useful for inductors as they can eliminate the need to gap the thin film core.

In terms of micro-transformers, the devices fabricated by the authors are predicted to have an efficiency of 78 % [21]. In order to increase the efficiency, significant improvements are required in the magnetic material. In particular, a high resistivity magnetic material (resistivity $> 150 \mu\Omega\text{cm}$) with high saturation flux density and low hysteresis loss is required. Alloys of CoNiFe, which have been reported to have a resistivity in the range 100 - 150 $\mu\Omega\text{cm}$, a saturation flux density in the range 1.6-1.9 T and a coercivity in the range 8 - 40 A/m [23] are promising solutions. Validated models of the fabricated micro-transformers can be used to determine the power densities and efficiencies achievable using the technology.

Section 4: Implications of Move to Magnetics on Silicon

From the above discussion, it is clear that thin film magnetics offer many advantages over conventional magnetics in terms of size and integration and, because of the high volume production benefits of silicon manufacturing, present a potential route to a low cost, high reliability magnetics technology platform that will be a key enabler for future PSOC applications. However, operating in the 5 to 10MHz frequency range presents significant challenges in the power and control area. Furthermore, reducing the size of the magnetics may be of little benefit if the capacitors remain discrete and bulky, and ultimately define the size of the final power system. A short commentary on these PSOC components is appropriate here and, while not exhaustive, does outline the current status and research challenges to be addressed in parallel with the development of magnetics-on-silicon.

Power Devices:

For cost and larger-scale integration reasons, it is desirable to implement PSoCs on mainstream CMOS/BiCMOS silicon processes. However, CMOS processes restrict the choice of power stage components. Available MOSFET devices typically include thin-oxide/mid-oxide lateral and DMOS structures, while the more area-efficient vertical MOSFETs are unavailable. While $R_{ds(on)}$ traditionally dominates the total power losses at low switching frequencies, the gate charge, Q_g , will become more dominant as the converter switching frequency is raised to multi-megahertz.

Lateral power devices have been reported that offer performance figures of merit, the product of the gate charge and $R_{ds(on)}$, that range from 2 to 3 times better than state-of-the-art trench MOSFETs [40]. Furthermore, as mentioned above, these devices can be fabricated with standard CMOS processes and thus result in great cost benefits and the potential to integrate control functions.

Control:

Power control blocks, implemented as active and passive components, are required to achieve good regulation of one or more converter variables (such as output voltage or input current), as well as housekeeping and functionality control (protection and interfacing) of the power converter. Traditionally, power converter control has been implemented using analogue continuous building blocks. However, it is anticipated by many experts that, for a variety of reasons, over the coming decade, most of these control building blocks will undergo a transition from analogue continuous towards digital discrete [29], [30], [31], [32].

Typical building blocks required by a digital power controller are ADCs, discrete controllers (either voltage or current programmed mode) and a digital pulse width modulator [29], [31], [32], [33], [34], [37], [38], [39]. Although IC solutions have been reported, the authors are the first to present a programmable DPWM IC architecture capable of producing flexible *PWM* pulse patterns supporting switching frequencies up to 15 MHz on standard CMOS that is compatible with silicon-integrated magnetics [36].

Capacitors:

The graph in figure 3 above showed the significant reductions in passive component values (between a factor of 5 and 20 times) that can be achieved as converter switching frequency is increased into the multi-megahertz region. In the illustrative example of the 3 Watt buck converter in Section 2, by 2008, at 10Mhz switching frequency, an output capacitance of 600nF has been estimated.

A typical 0.35um CMOS foundry process, with a gate-oxide thickness in the region of 5-10nm, will provide poly-diffusion capacitances of about 5nF/mm². A 600nF capacitance would require an area of 11 by 11 mm using this material. Voltage-stable poly-poly capacitances will only provide 1nF/mm² (at an oxide thickness of around 40nm). While not available widely yet in standard foundry processes, thin-oxide metal-metal capacitances (i.e. MIM – metal-insulator-metal) using silicon dioxide, (SiO₂), silicon nitride (Si₃N₄) or tantalum pentoxide (Ta₂O₅), with dielectric constants of 3.9, 7 and 25 respectively, will deliver capacitance values of 1, 2 and 5nF/mm² respectively. In the context of using standard semiconductor processes, Ta₂O₅ MIM capacitors have been integrated at the level of Al-interconnections in BiCMOS technologies [41],[42]. For very high dielectric constant materials (i.e. 1000 to 2000 in thin film form), PMNT relaxor ferroelectrics offer silicon integrated capacitor

structures with capacitance values in the range 20 to 40nF/mm² [43] suggesting that the required 600nF capacitance could be achieved in an area of between 4 and 5mm square.

System Integration / Functional Integration

The concept of power system in a package (PSIP) has been used extensively in surface mount power supply modules. In fact, it can be argued that board mounted power supplies (BMPS) are in fact in a PSIP format. It is also evident that the main driver to power supply evolution over the last decade has been silicon integration with the resulting BMPS trend from quarter brick to 1/16th brick delivering higher power densities and reliability at lower cost per watt, through an ongoing increase in converter efficiency and a reduction in component count. However, while these PSIP products present, to the end-user, a single, surface-mountable, component solution, they still contain a number of discrete active and passive components assembled on a multi-chip substrate with resultant impact on product reliability and cost.

Moving beyond the PSIP, the subject of this paper, magnetics-on-silicon, presents an opportunity to create the ultimate solution, a chip-scale, power system-on-a-chip or power supply-on-a-chip (PSOC), a chip-scale package (CSP) incorporating a monolithic chip with functional integration of the power, control, magnetics and capacitors. Key material and manufacturing technologies that are required to enable this evolution include wafer-scale processing of magnetics-on-silicon and 3-D stacking of magnetics and capacitors on a power ASIC. Developing these materials and/or technologies represent the key research challenges for integration in moving to the ultimate PSOC.

Section 7: Conclusions

Trends from semiconductor technology roadmaps show the need to move to multi-megahertz switching power converters in order to minimise the values, and therefore the size, of passive components. This opens the opportunity to consider the integration of magnetics on silicon which enables the concept of power supply on chip (PSOC), the ultimate in power supply miniaturisation and functional integration. This will require a move away from conventional ferrite materials to semiconductor compatible processing of magnetic materials based on electroplating or sputtering of multilayer thin film permalloys. Magnetics-on-silicon technology has demonstrated inductances up to 1microH at 5MHz, dc resistances as low as 150milliOhms and Q up to 18. Load currents up to 10Amps have been demonstrated for coupled inductors.

Technical challenges associated with magnetics on silicon that need to be addressed include magnetic materials with reduced losses and reduced resistance conductors or windings. Multi-megahertz converters also will require other components to be compatible that include power switches, digital control circuits and integrated capacitors. A key challenge will be to achieve the integration using standard CMOS/BiCMOS.

Section 6: Acknowledgements

The authors gratefully acknowledge funding from Enterprise Ireland for the research described here.

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